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MICROWAVE SOLID-STATE DEVICE AND CIRCUIT STUDIES

The University of Michigan

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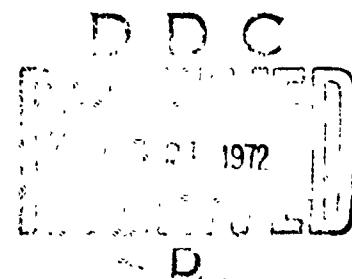
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FOREWORD

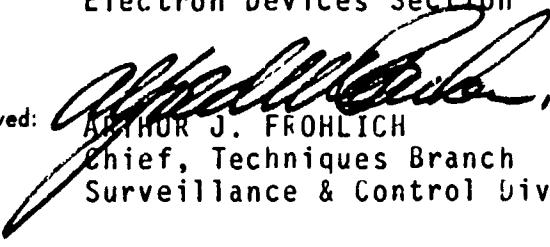
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This report has been reviewed and is approved.

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ABSTRACT

The equivalent circuit representation of the WR-90 waveguide resonant circuit with post mounting of devices is used to analyze the RF loads presented to X-band Gunn-effect devices. Experimental data for a pulsed oscillator is analyzed over the frequency range of 8 to 12 GHz. Domain mode behavior is found.

Calculated bandwidths of the order of an octave are shown for stabilized transferred-electron amplifiers using short crystal lengths. Effects of lattice temperature on the behavior of these devices are described. The possibility of improving the dc to RF conversion efficiency by a lattice temperature gradient, or by a doping gradient along the length of the GaAs crystal is discussed.

The frequency modulation sensitivities of a Gunn-effect device mounted in a coaxial circuit is measured for different lattice temperatures and bias values. The rapid changes in modulation sensitivity are shown to be due mainly to device changes and not RF circuit properties. In addition, the circuit parameters that limit the electronic tuning rate of the device in a waveguide circuit are found.

Equivalent circuits for the diode package transformation in 50Ω microstrip line and in ridged waveguide are presented, the method for their determination is discussed and admittance characteristics for GaAs and Si diodes biased at 1000 A/cm^2 are given.

Further development of the computer program modeling of the IMPATT mode of the avalanche-diode oscillator has been carried out which has resulted in a significant improvement of its rate of convergence. A program to calculate independently the small-signal admittance for an arbitrary doping profile has also been written. A description is given of the approach to be taken to permit modeling of the TRAPATT mode.

Some representative numerical results obtained from a large-signal IMPATT diode computer analysis are presented and discussed.

An improved diode fabrication process is described. A group of diodes with low thermal resistance has been obtained. IMPATT diodes fabricated with the process have been tested with powers in the 100 to 600 mW range (CW) and with frequencies between 6.5 and 8.5 GHz.

A variable step size numerical integration scheme has been implemented for calculating the collision integrals in the dc analysis of germanium. Modifications are being made in the computer program so that this scheme does not take excessive computer time.

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PUBLICATIONS DURING THE LAST QUARTER

W. E. Schroeder and G. I. Haddad, "The Effect of Temperature on the Operation of an IMPATT Diode," Proc. IEEE (Correspondence), vol. 59, No. 8, pp. 1242-1244, August 1971.

W. E. Schroeder and G. I. Haddad, "Avalanche Region Width in Various Structures of IMPATT Diodes," Proc. IEEE (Correspondence), vol. 59, No. 8, pp. 1245-1248, August 1971.

W. E. Schroeder, C. M. Lee, R. J. Lomax and G. I. Haddad, "Avalanche Region Width in Various Structures of IMPATT Diodes," Presented at the 1971 Device Research Conf., Ann Arbor, Mich., June 28-July 1, 1971.

A. K. Talwar and W. R. Curtice, "A Study of Stabilized Transfer-Electron Amplifiers," Presented at the 1971 Cornell Conf. on High Frequency Generation and Amplification: Devices and Applications, Ithaca, New York, August 1971.

R. W. Laton and G. I. Haddad, "The Effects of Doping Profile on Reflection-Type IMPATT Diode Amplifiers," Presented at the 1971 European Microwave Conf., Stockholm, Sweden, August 1971.

MICROWAVE SOLID-STATE DEVICE AND CIRCUIT STUDIES

1. General Introduction (G. I. Haddad)

The research under this program is concerned with investigation and utilization of various phenomena and techniques for the generation, amplification and detection of electromagnetic energy at microwave frequencies. The work is oriented mainly toward an investigation of the basic properties of avalanche transit-time and transferred-electron devices and the incorporation of these devices in various types of circuits including microstrip.

Several tasks were active during this period. The status of each and the work planned for the next period are discussed in detail in the following sections of this report.

2. High-Power Gunn-Effect Devices (W. R. Curtice)

2.1 Introduction. Many previous experiments with pulsed and CW Gunn-effect (or transferred-electron) oscillators produced data inconsistent with domain mode theory. The most puzzling aspect was the inability to tune devices over a wide frequency range with good efficiency in the Q-mode (quenched-domain mode). Part of this difficulty was due to RF circuit problems, that is, the inability to present proper impedance to the TE device. The waveguide circuit analysis and pulsed oscillator characteristics described in this report will enable a better understanding of these frequency tuning problems.

2.2 RF Circuit Characteristics. The equivalent circuit representation for the WR-90 waveguide circuit with post mounting of devices was

presented in the last quarterly progress report. The physical circuit consists of a 0.1-inch diameter post centered in the waveguide and touching a TE device at one wall. An adjustable waveguide short is behind the post. An RF bypass capacitor exists at one end of the post so that device bias can be applied through the post. The package parameters of the TE device are included in the equivalent circuit.

Figures 2.1 and 2.2 show the calculated load resistance and reactance presented to the TE device for a shorting plane position 2.354 cm from the post and for three different waveguide load conditions. Z_L is the waveguide load at the plane of the post. The load conditions are Z_0 (matched), $1/2 Z_0$ and $2 Z_0$. The second and third load conditions can be obtained with a slide-screw tuner of VSWR equal to 2.0 at a proper distance from the post. Figure 2.2 shows that for a matched load the circuit exhibits a series resonance at 8.802 GHz and a parallel resonance at 9.062 GHz. The circuit is inductive only between these frequencies in X-band. Oscillation with the capacitive TE device M61-24 occurs around 9.01 GHz. At this frequency both load resistance and reactance change considerably with change of the external real load value.

Figure 2.3 shows the load admittance for the same circuit and shorting plane position and for the same external loads. The admittance presentation has been found to be more useful for TE device analysis. Note that oscillation occurs closest to the frequency of parallel circuit resonance.

Figure 2.3 can be used to evaluate the circuit factor R_0/Q_0 from the equation

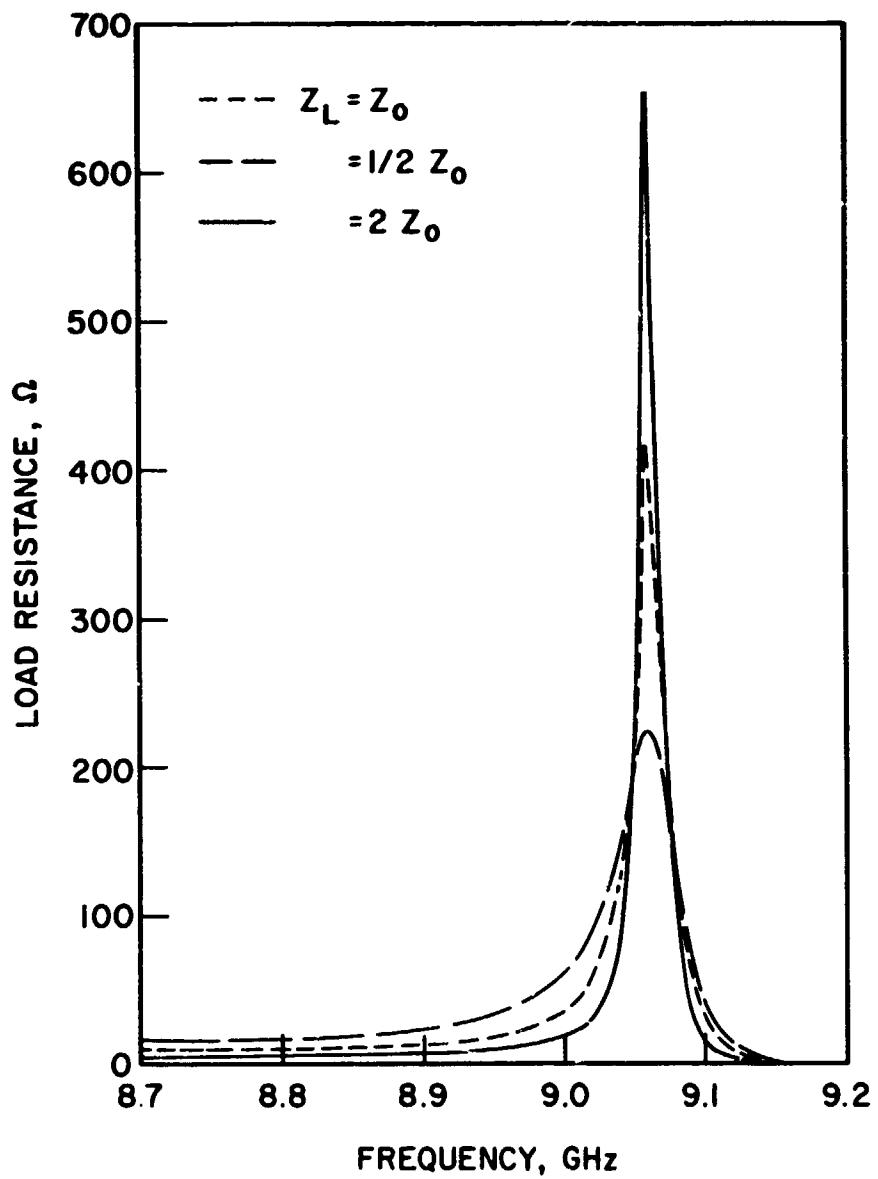


FIG. 2.1 LOAD RESISTANCE PRESENTED TO THE TE DEVICE IN THE WAVEGUIDE CIRCUIT AS A FUNCTION OF FREQUENCY. SHORT PLANE IS 2.354 cm FROM THE POST.

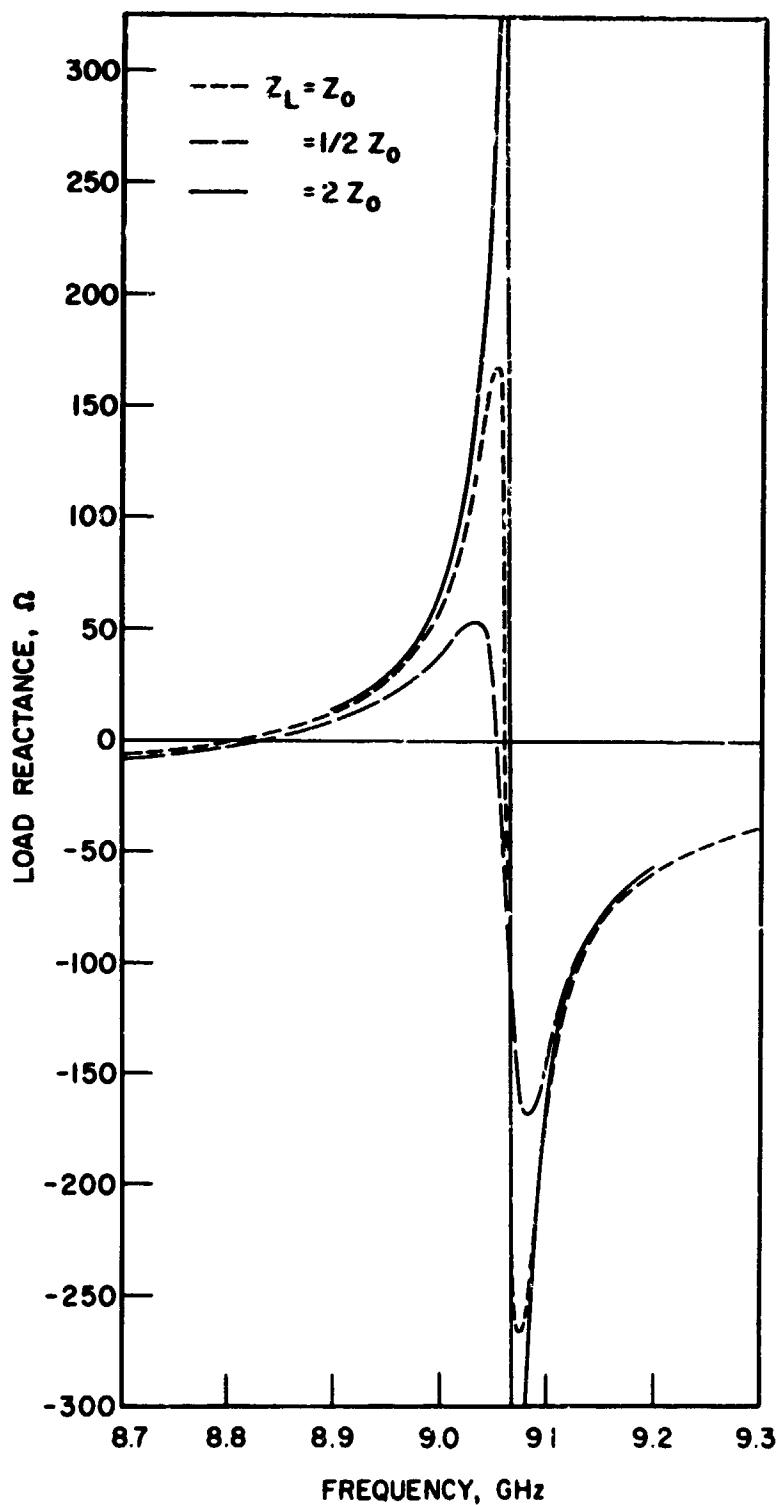


FIG. 2.2 LOAD REACTANCE PRESENTED TO THE TE DEVICE AS A FUNCTION OF FREQUENCY IN THE WAVEGUIDE CIRCUIT. SHORT PLANE IS 2.354 cm FROM THE POST.

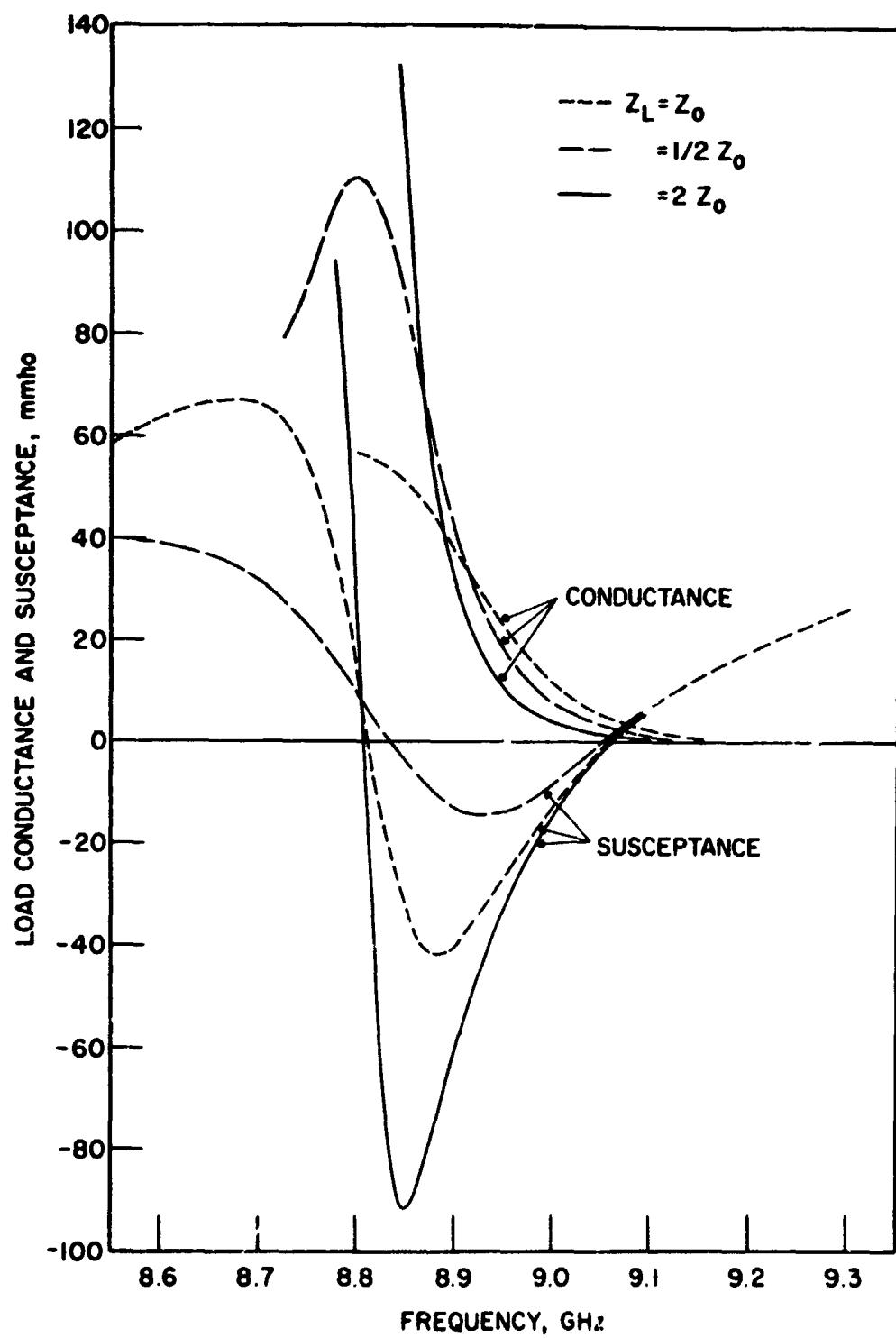


FIG. 2.3 LOAD ADMITTANCE PRESENTED TO THE TE DEVICE IN THE WAVEGUIDE CIRCUIT AS A FUNCTION OF FREQUENCY. SHORT PLANE IS 2.354 cm FROM THE POST.

$$\frac{\Delta f}{f_o} = -\frac{1}{2} \Delta B \left(\frac{R_o}{Q_o} \right) .$$

The R_o/Q_o factor for the matched circuit is 0.994Ω while it is 1.53Ω and 0.868Ω for loads of $1/2 Z_o$ and $2 Z_o$, respectively. The external Q factor Q_x was evaluated for the matched load condition and found to be 200. The load conductance estimate used in earlier work of $(R_o/Q_o \cdot Q_x)^{-1} \approx 0.005$ mho (at 9.01 GHz) is only a little different from the actual load conductance of 0.006 mho. However, the load conductance changes so rapidly with frequency that this method of calculation is not reliable. An ideal parallel resonant circuit would have nearly constant (device) load conductance around resonance.

Oscillation ceases for low bias on the TE devices and the reason for this is the real loading change. As the bias is lowered, the device susceptance increases which, as shown in Fig. 2.3, lowers the frequency of oscillation. The real load increases as the frequency is lowered and finally becomes too large to sustain the circuit controlled oscillation.

Calculations for matched load conditions and for a closer short plane position show much larger load conductance values for the same values of load susceptance. Thus without an external tuner, the device real load is greatly increased for higher frequency operation. Figure 2.4 shows admittance calculations for a closer short plane position and matched load. It is seen that load conductance is increased at parallel resonance and the separation between series and parallel resonant frequencies has also increased greatly. The R_o/Q_o value at 10.5 GHz is 1.45 which is not greatly different from the value for lower resonant frequencies.

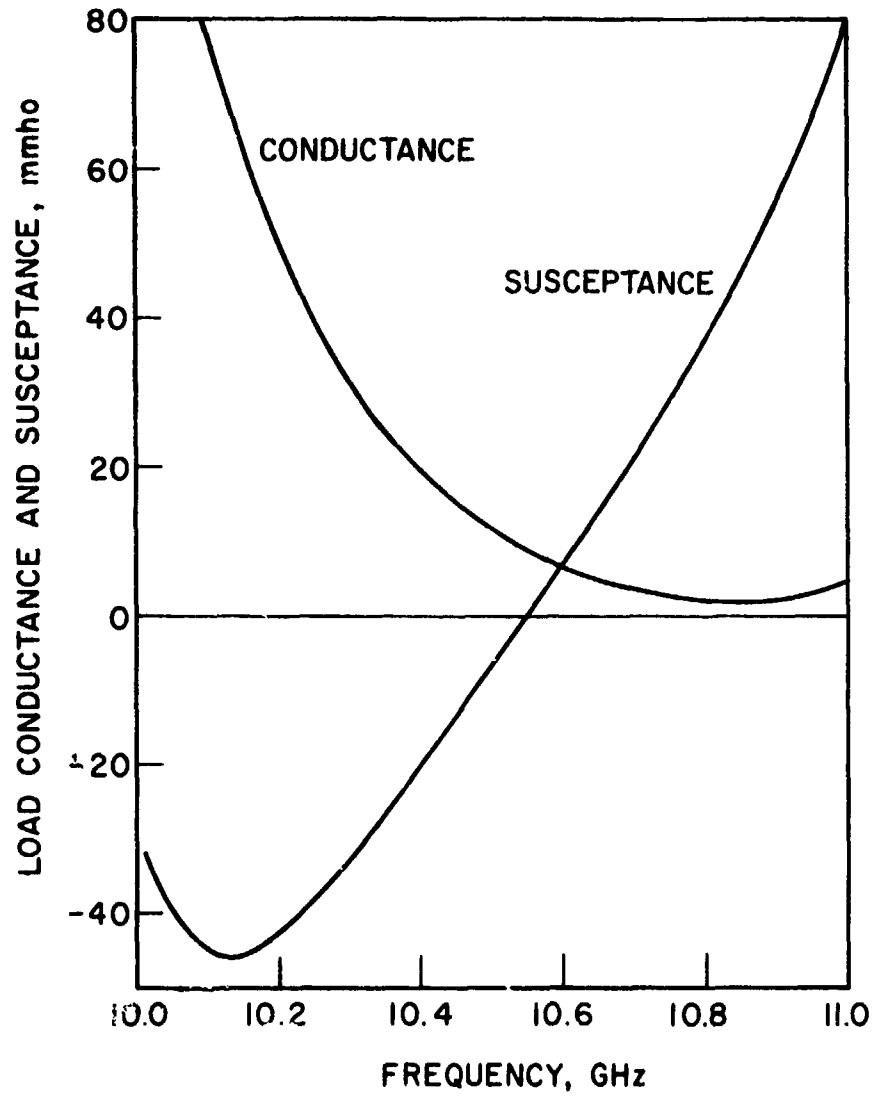


FIG. 2.4 LOAD ADMITTANCE PRESENTED TO A TE DEVICE IN THE WAVEGUIDE CIRCUIT AS A FUNCTION OF FREQUENCY. SHORT PLANE IS 1.735 cm FROM THE POST.

Figure 2.5 shows how the real load increases with increase of the circuit resonant frequency (by decrease of the post-to-short plane separation). It is clear from this data that for the same values of circuit susceptance, the load conductance increases strongly with increase of resonant frequency. This is the reason for the poor TE device performance without a tuner at high frequencies. The increased loading causes a power decrease with frequency and does not allow oscillation above 11 GHz.

2.3 Experiments with a Pulsed TE Device in the Waveguide Circuit.

Preliminary tests of TE device M61-24 were described in the last quarterly progress report. The device has the following parameters:

$$n_0 = 2 \times 10^{15} / \text{cm}^3,$$

$$l = 13.7 \text{ } \mu\text{m},$$

$$\mu_H = 0.75 \text{ m}^2/\text{V-s},$$

$$\text{area} \approx 10^{-4} \text{ cm}^2,$$

$$V_{TH} = 4.45 \text{ V.}$$

$$I_{TH} = 0.525 \text{ A (low duty operation) and}$$

$$R_{\text{low field}} = 5.52 \text{ } \Omega.$$

The pulsed power output obtained for TE device M61-24 in the waveguide circuit is shown in Fig. 2.6 for operation with a slide-screw tuner and for a matched load. For the matched load condition, the device admittance can be calculated from the frequency of oscillation using the known equivalent circuit. The RF voltage can be obtained from the RF power value and the real load presented to the device. These results are presented in Fig. 2.7 for operation at 15 V bias. The increased device loading with frequency not only reduces the RF power but also reduces the RF voltage.

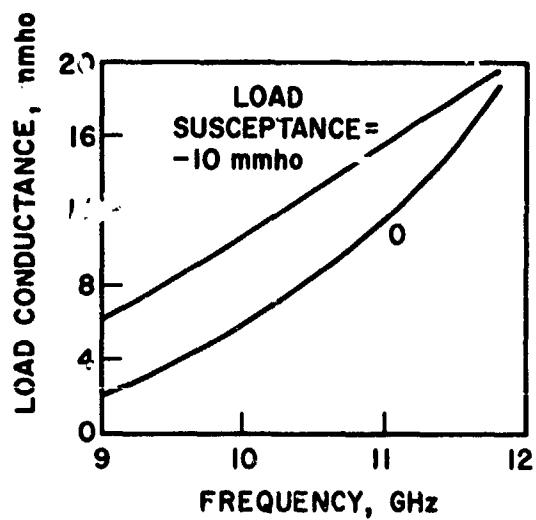
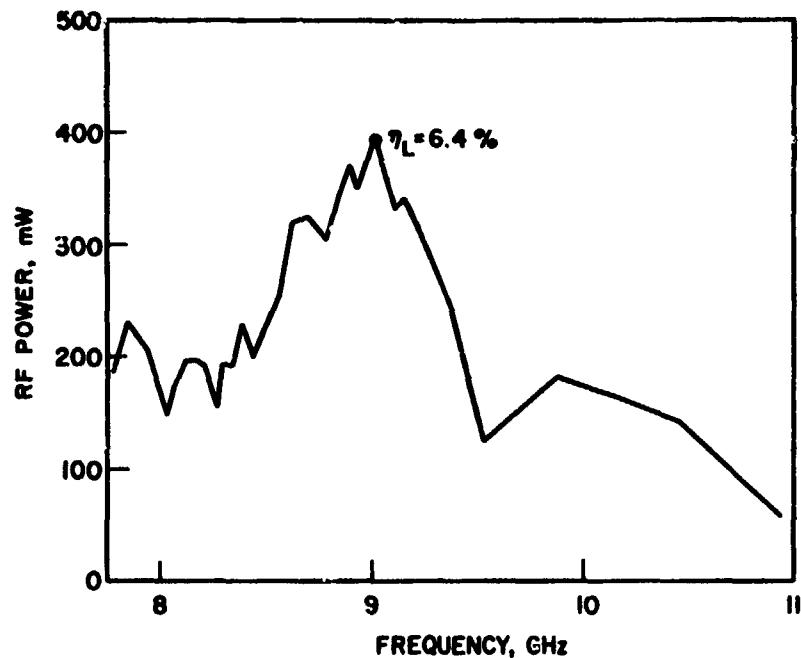
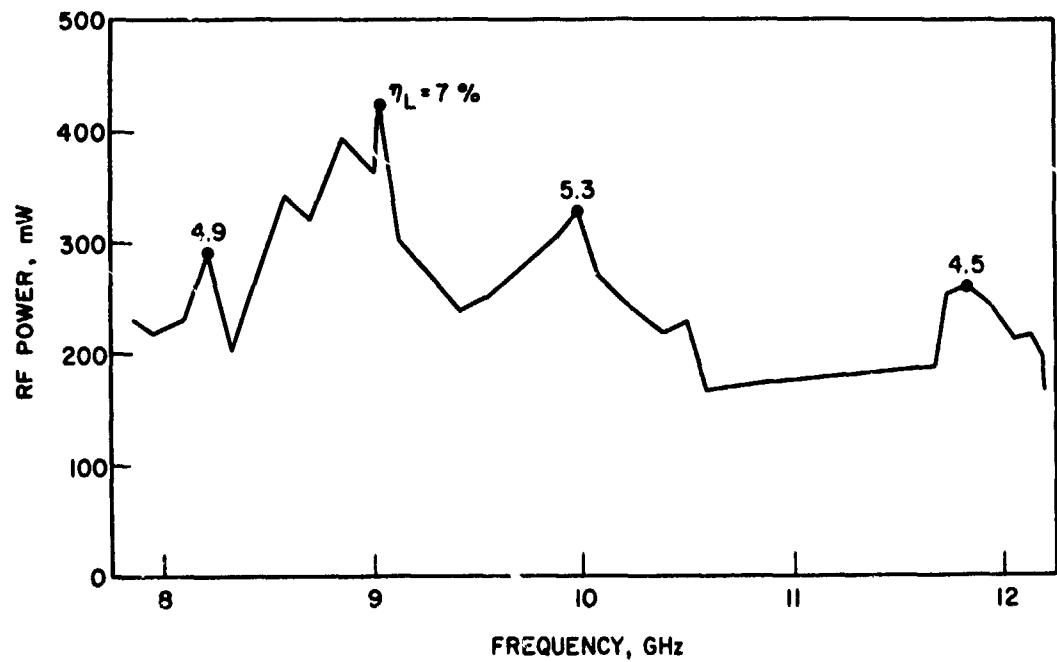


FIG. 2.5 LOAD CONDUCTANCE AS A FUNCTION OF RESONANT FREQUENCY FOR MATCHED WAVEGUIDE CIRCUIT FOR TWO VALUES OF LOAD SUSCEPTANCE.



(a) MATCHED LOAD CONDITION



(b) SLIDE-SCREW TUNER USED TO MAXIMIZE OUTPUT POWER

FIG. 2.6 PULSED RF POWER OUTPUT AS A FUNCTION OF FREQUENCY FOR TE DEVICE
M61-24 IN THE WAVEGUIDE CIRCUIT. ($V_B = 15$ V)

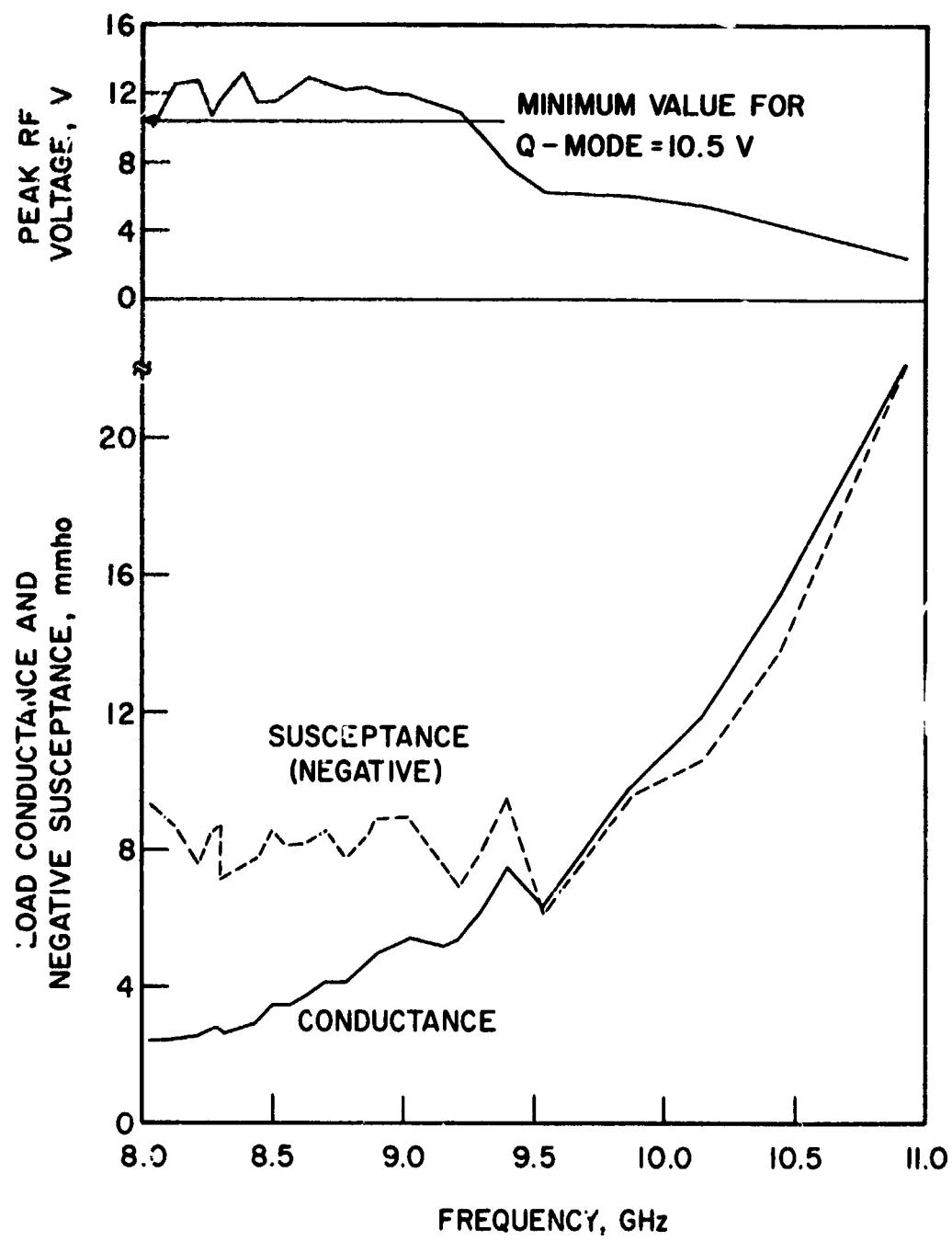


FIG. 2.7 RF VOLTAGE, LOAD CONDUCTANCE AND SUSCEPTANCE AS A FUNCTION OF FREQUENCY OF OSCILLATION FOR PULSED TE DEVICE M61-24 IN THE WAVEGUIDE CIRCUIT WITHOUT A TUNER AND WITH 15 V BIAS.

Operation above 9.25 GHz occurs with RF voltages insufficient for single-frequency Q-mode. In fact, any RF voltage value between 2 and 13 V seems to be allowable.

The load presented to the TE device with and without a tuner are shown in Fig. 2.8 for 15 V bias. The matched load results are slightly different from the values in Fig. 2.7 because a correction was made for a slight mismatch ($VSWR < 1.2$) in the load line which was found to be present during the tests. For measurements with a tuner, the actual waveguide load admittance was measured after adjustment of the tuner for best RF power output.

Notice that the load susceptance is nearly the same for the two cases in Fig. 2.8, but that the load conductance is significantly lower at high frequencies for operation with the tuner. The RF voltage differences existing in the two cases mainly affect the device conductance and not the susceptance.

Figures 2.9 and 2.10 show the TE device admittance, RF voltage and capacitance as a function of frequency for optimum load (with tuner) and for two bias values. The device capacitance is calculated from susceptance and is seen to decrease with bias increase and shows a tendency to increase with frequency. The RF voltages are larger than for the matched load case (Fig. 2.7) but still are insufficient for Q-mode over a portion of X-band in both cases.

Figure 2.11 shows the TE device characteristics near 9 GHz for various values of bias. A decrease in conductance and susceptance clearly occurs for increasing bias values. Furthermore RF voltage is sufficient for Q-mode at each value of bias.

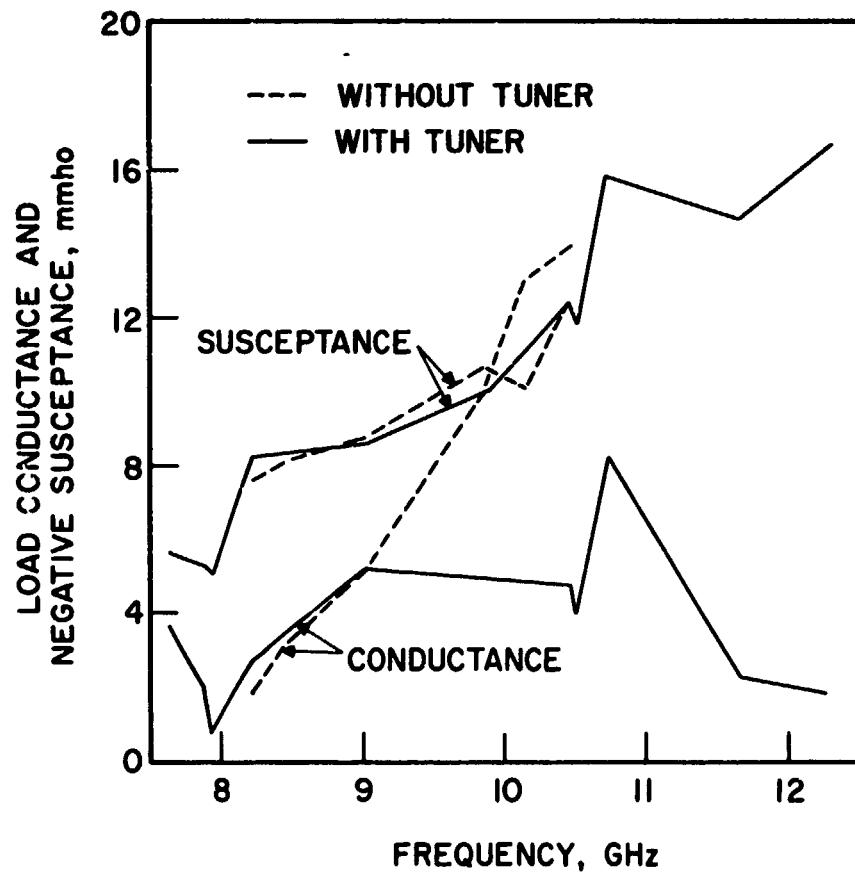


FIG. 2.8 LOAD CONDUCTANCE AND SUSCEPTANCE VS. FREQUENCY FOR TE DEVICE M61-24 FOR THE MATCHED LOAD CASE AND FOR THE BEST RF POWER CONDITION USING AN RF TUNER IN LOAD LINE. ($V_B = 15$ V)

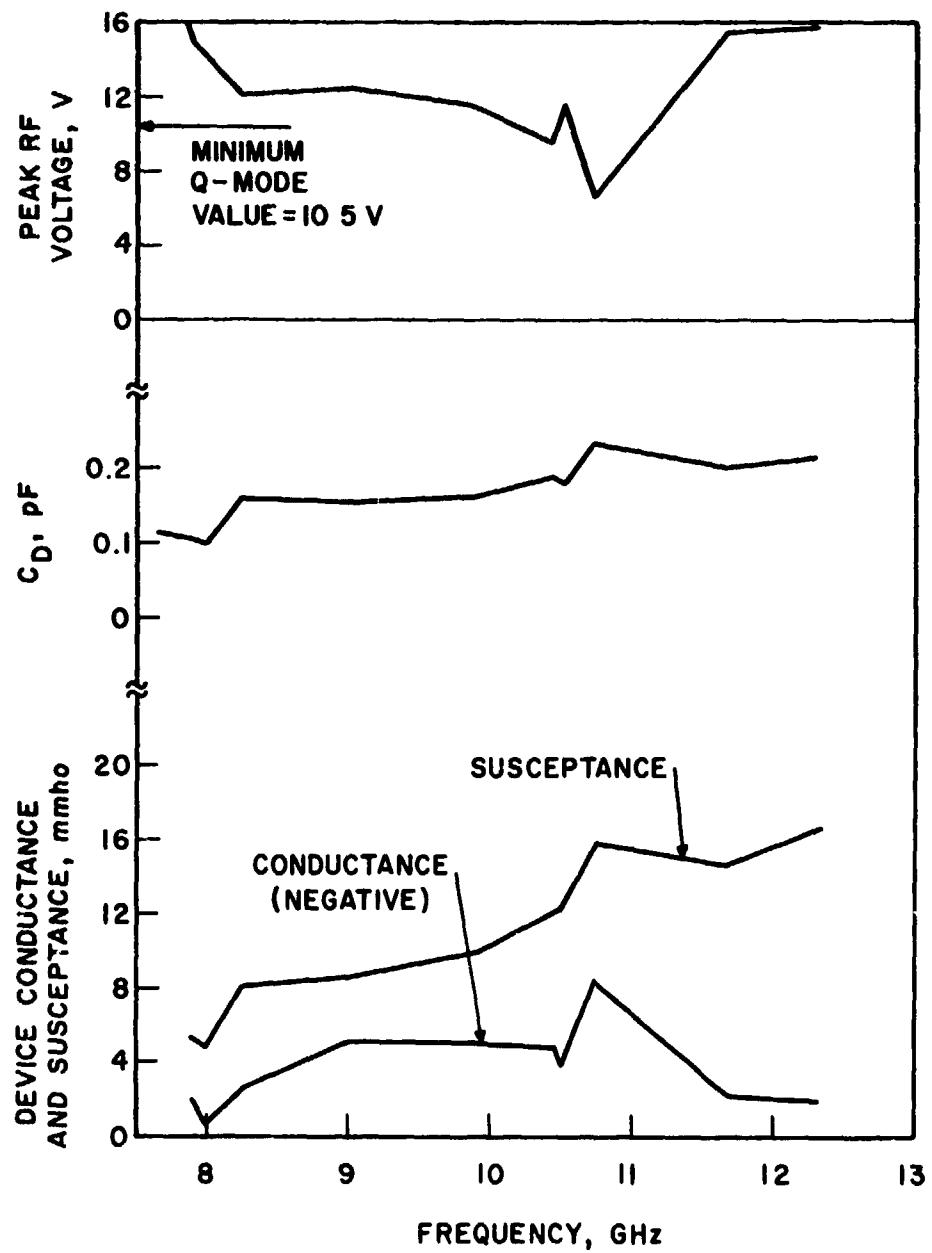


FIG. 2.9 ADMITTANCE, CAPACITANCE AND RF VOLTAGE AS A FUNCTION OF RF FREQUENCY FOR TE DEVICE M61-24 IN THE WAVEGUIDE CIRCUIT WITH A TUNER FOR BEST OUTPUT POWER. ($V_B = 15$ V)

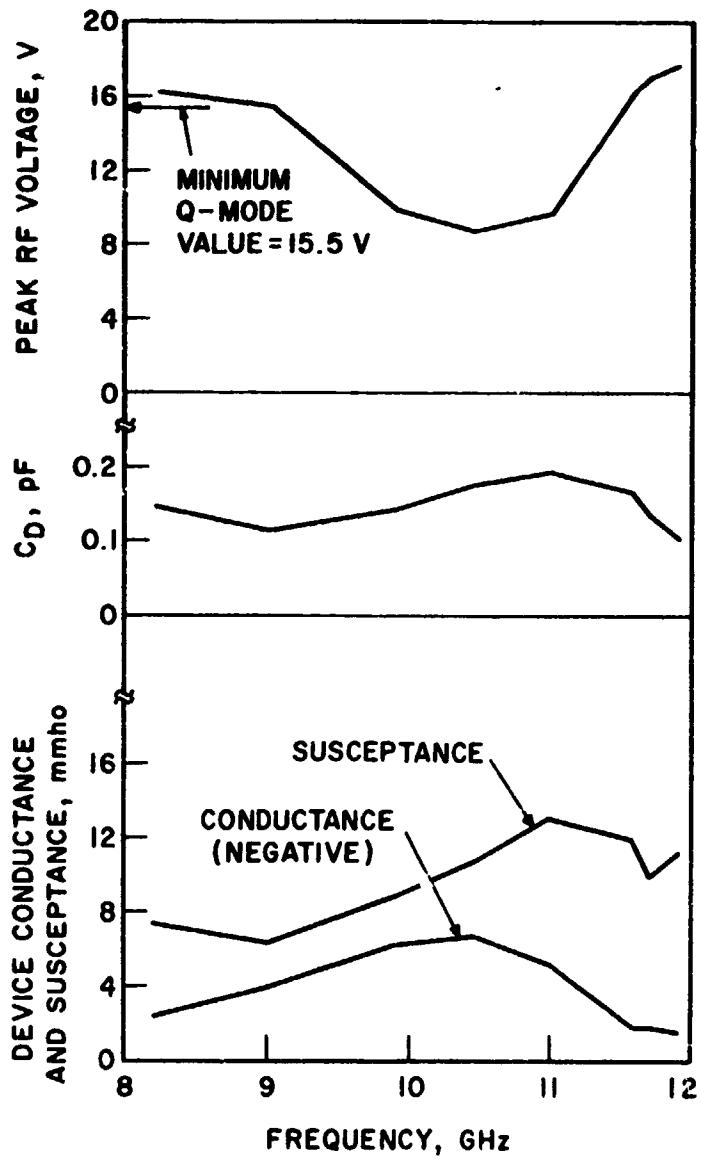


FIG. 2.10 ADMITTANCE, CAPACITANCE AND RF VOLTAGE AS A FUNCTION OF RF FREQUENCY FOR TE DEVICE M61-24 IN THE WAVEGUIDE CIRCUIT WITH A TUNER FOR BEST OUTPUT POWER. ($V_B = 20$ V)

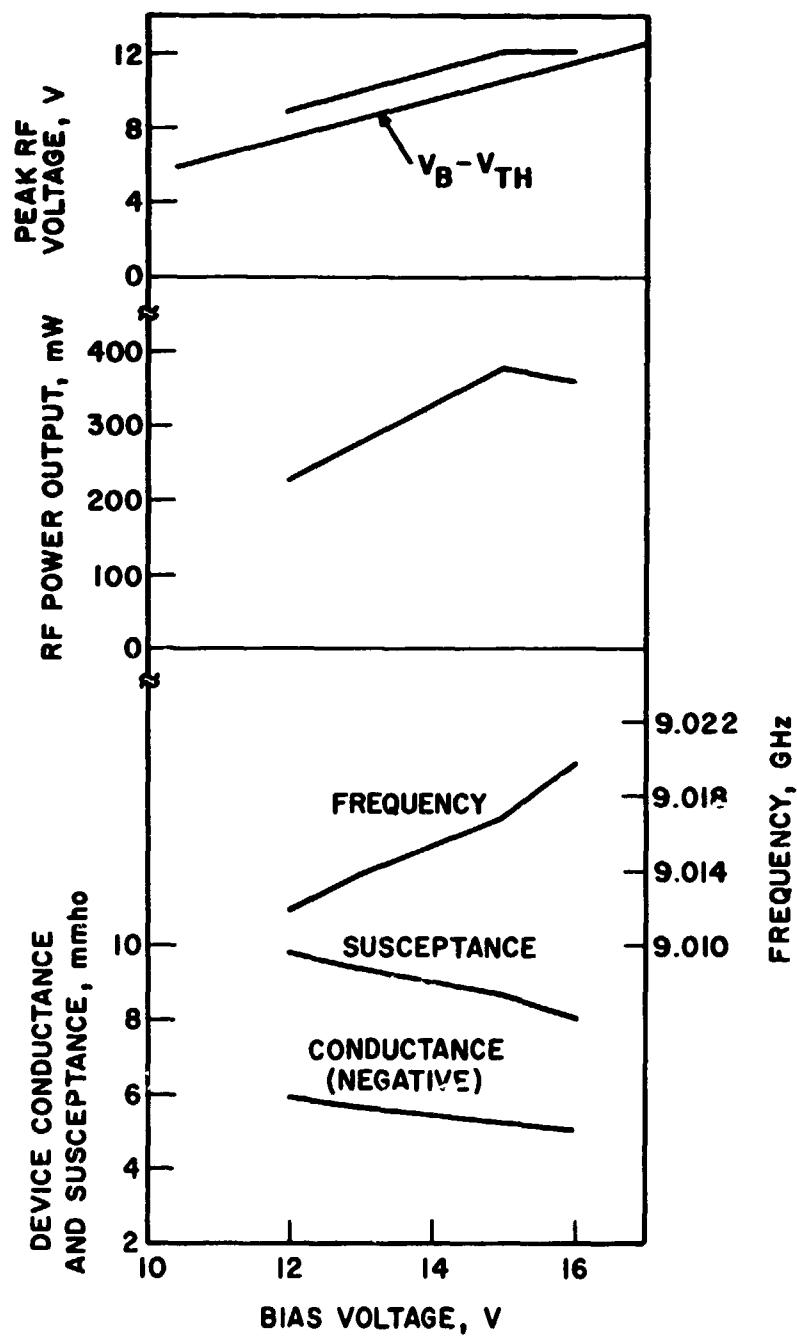


FIG. 2.11 RF POWER OUTPUT, FREQUENCY OF OSCILLATION, RF VOLTAGE, LOAD CONDUCTANCE AND SUSCEPTANCE AS A FUNCTION OF BIAS VOLTAGE FOR TE DEVICE M61-24 IN THE WAVEGUIDE CIRCUIT WITHOUT A TUNER AND FOR A POST-TO-SHORT DISTANCE OF 2.354 cm.

2.4 Conclusions. Analysis of the post-type WR-90 waveguide circuit has shown that for post-to-short plane separations close to one-half wavelength only one circuit resonance occurs in X-band for capacitive Gunn devices. This occurs above a frequency of series resonance and slightly below a frequency of parallel resonance. For a matched load condition, the real loading of the TE device increases greatly for an increase of circuit resonant frequency. This is responsible for the observed power falloff with frequency for TE device M61-24. Use of a slide-screw tuner was shown to result in lower load conductance and larger RF power over all of X-band.

Careful measurements of device admittance and RF voltage verified the preliminary data obtained by other methods and reported in previous quarterly progress reports. In particular, RF voltage is found to be sufficient for Q-mode operation only when load conductance is reduced to values nearly optimum for best RF power output. It is possible that harmonic voltages aid the quenching process for the higher load condition.

The operating characteristics at 15 V bias and below are most consistent with Q-mode behavior. Operation at higher voltages probably involves incomplete domain formation. Characterization of the active diode as a parallel capacitor and a negative resistor is appropriate over a wide frequency range. For fixed voltage bias, the capacitance is not a strong function of frequency or RF voltage. The capacitance reduces as bias is increased and is about twice the low-field value at 20 V which is 4.5 times threshold. This result is consistent with Q-mode theory. The magnitude of the device negative conductance decreases with increase of either bias voltage or RF voltage.

2.5 Program for the Next Quarter. The experimental study of pulsed and CW TE oscillators will be continued. The circuit-device interaction problem will be studied in an effort to understand why RF efficiency varies so much as a function of frequency.

2. Gunn-Effect Amplifiers

Supervisor: W. R. Curtice

Staff: A. K. Talwar

3.1 Introduction. In Quarterly Progress Report No. 3, numerically calculated results of a large-signal analysis of stabilized transferred-electron devices were given. The dependence of impedance and efficiency upon RF signal amplitude and length of the device, etc., was described. Effects of diffusion were also discussed. In this report, plots of small- and large-signal impedance against frequency are shown in order to enable an assessment of the bandwidth capabilities of these devices. Nearly octave bandwidths as observed experimentally by Perlman¹ have been calculated. It is also shown in this report that inclusion of field dependence of diffusion is essential for an accurate evaluation of the dc characteristics of these devices. The effects of lattice temperature on the various characteristics of these devices is investigated. It is shown that a rise in lattice temperature does not necessarily reduce the magnitude of negative resistance. Sufficient increase in lattice temperature above the room temperature may be necessary for significant reduction of the magnitude of negative RF resistance in order to aid stabilization of the devices. The

1. Perlman, B. S., "Microwave Amplification Using Transferred-Electron Devices in Prototype Filter Equalization Networks," RCA Rev., vol. 32, No. 1, pp. 3-23, March 1971.

effects of gradients in lattice temperature and donor density along the length of a stabilized GaAs crystal are discussed analytically. It is suggested that such gradients can have significant influence on the performance of these devices. In particular, RF to dc conversion efficiency can be improved by properly controlling such gradients.

3.2 Bandwidth Considerations. Figure 3.1 shows the resistance and reactance of a 14- μm long crystal with $n_0 = 5 \times 10^{14}/\text{cm}^3$ plotted as a function of frequency for different values of normalized RF current. As before, the currents are normalized with respect to J_{th} as

$$J_{\text{th}} = n_0 e v_{\text{th}} , \quad (3.1)$$

where v_{th} is the carrier velocity at the threshold electric field, J_c is taken to be 10 percent above J_{th} and the area was taken to be $9.8 \times 10^{-4} \text{ cm}^2$.

The impedance results show two negative resistance frequency regions which may be used for reflection amplification. The low-frequency region occurs near the transit-time frequency since 6 GHz times 14 μm is $0.84 \times 10^7 \text{ cm/s}$. Note here that the reactance is about twice the value of (negative) resistance. This relationship influences the gain-bandwidth product when the device is used for amplification.

$J_{11} = 0.001$ is a small-signal case, since any value less than this leads to the same results. It is seen that the maximum negative resistance at first increases, as J_{11} is increased, and then decreases. Figure 3.2 shows a plot similar to that of Fig. 3.1 for a crystal with the same donor density, but with a length of 10 μm and an area of $7 \times 10^{-4} \text{ cm}^2$. The low-field resistance is kept the same (nearly 2.5Ω) in the two cases. The dc current density is also the same. The shorter device (Fig. 3.2)

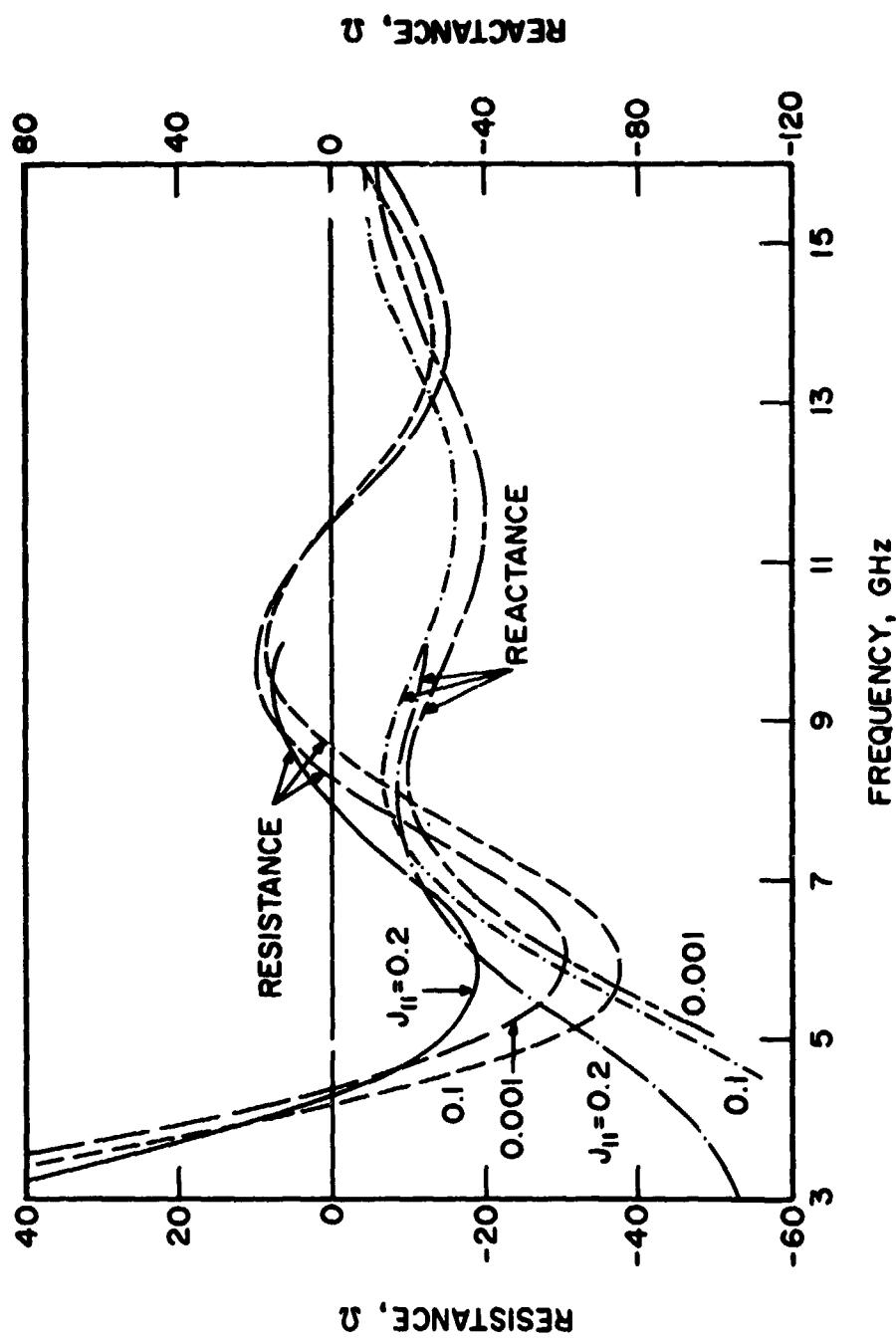


FIG. 3.1 IMPEDANCE AS A FUNCTION OF FREQUENCY AT 300°K WITH DIFFUSION EFFECTS INCLUDED.
 $(n_0 = 5 \times 10^{14}/\text{cm}^3$, LENGTH = 14 μm , $J_0 = 1.1$ AND AREA = $9.8 \times 10^{-4} \text{ cm}^2$)

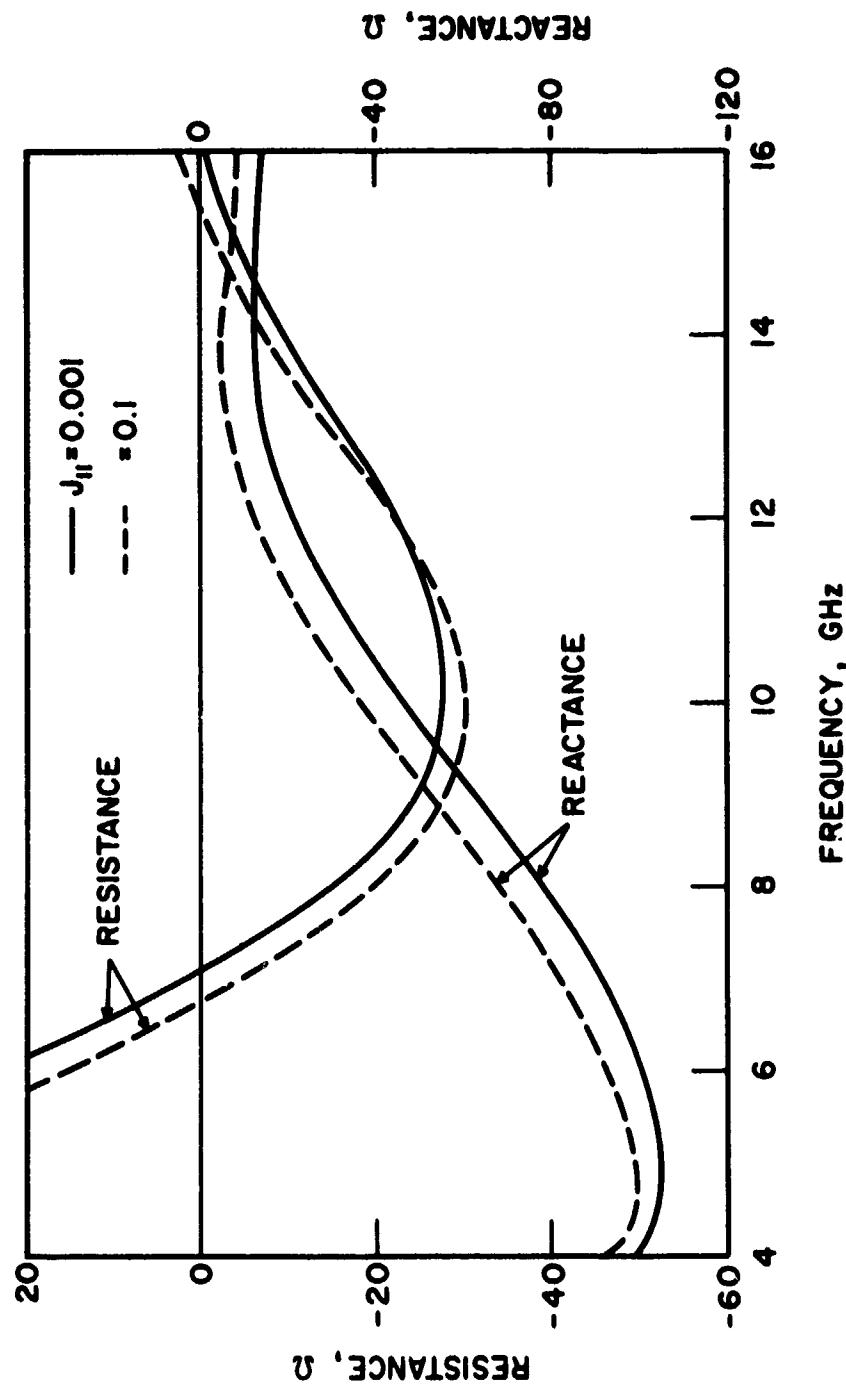


FIG. 3.2 IMPEDANCE AS A FUNCTION OF FREQUENCY AT 300°K WITH DIFFUSION EFFECTS INCLUDED. ($n_0 = 5 \times 10^{14}/\text{cm}^3$, LENGTH = 10 μm , $J_0 = 1.1$ AND AREA = $7 \times 10^{-4} \text{ cm}^2$)

has a slightly smaller magnitude of negative resistance. As expected, the negative resistance frequency region is shifted to higher frequencies. The frequency range of this region is larger than that for the longer device. The last result seems to agree with the calculations of Magarshak and Mircea² who have found very large bandwidths for short crystals. The shapes of the resistance and reactance plots of Figs. 3.1 and 3.2 bear a marked resemblance to the experimental curves of Perlman.¹

3.3 Field Dependence of Diffusion Coefficient and Its Importance in Determining the dc Characteristics Accurately. The calculated value of average carrier density n , and the values of diffusion coefficient corresponding to the average electric field at each point along the length of the crystal of Fig. 3.1 are plotted in Fig. 3.3 for a small RF signal level. Note that the dc current due to a gradient in carrier density and that due to a gradient in diffusion coefficient flow in opposite directions. Thus the assumption of a field-independent, constant diffusion coefficient would lead to erroneous results. Clearly, a more accurate dc solution is obtained if the diffusion is neglected completely than if it is taken to be a constant. Of course, taking into account the field dependence of the diffusion coefficient gives the most accurate results.

3.4 Effects of Lattice Temperature. In this section it is assumed that the lattice temperature is the same everywhere inside the crystal. An increase in lattice temperature reduces both the low-field mobility and the negative differential mobility and changes the static field profile in

2. Magarshak, J. and Mircea, A., "Wideband CW Amplification in X-Band with Gunn Diode," Int. Solid State Circuits Conf. Digest, Philadelphia, Pa., p. 134, February 1970.

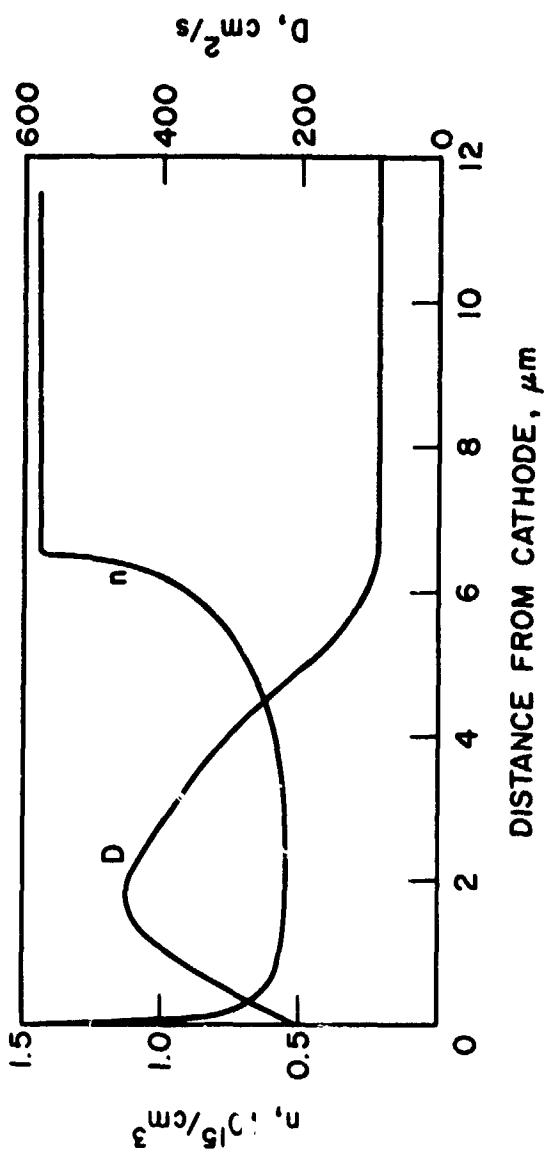


FIG. 3.3 AVERAGE CARRIER DENSITY AND DIFFUSION COEFFICIENT VS. DISTANCE FROM THE CATHODE AT 300°K WITH DIFFUSION EFFECTS INCLUDED. ($n_0 = 5 \times 10^{14}/\text{cm}^3$, $J_0 = 1.1$, $J_{11} = 0.001$ AND FREQUENCY = 10 GHz)

the crystal. In order to understand the effects of these changes, small-signal impedance calculations³ were made assuming a piece-wise linear v-E characteristic and $D = 0$. Figure 3.4 shows the different v-E relationships used and these have different peak-to-valley ratios. Computations were made for a crystal of $10 \mu\text{m}$, $n_0 = 5 \times 10^{14}/\text{cm}^3$ and $a_{\text{an},\text{a}} = 7 \times 10^{-4} \text{ cm}^2$ over a band of frequencies and the maximum negative resistance obtained (around 10 GHz) is plotted against peak-to-valley ratios in Fig. 3.5 for a value of J_0 equal to 1.1. Maximum value of negative resistance in the frequency band is chosen so that transit angle effects are unimportant for the following discussion. Although a direct decrease in the magnitude of negative resistance with a decrease in the peak-to-valley ratio was expected, it did not always occur. Instead, the maximum negative resistance was not greatly affected by changes in the peak-to-valley ratio unless the ratio was small. The reason for this behavior can be explained with the aid of Fig. 3.5 which shows the values of L_n , the length of the active region, and L_a , the length of the anode region. A large peak-to-valley ratio results in a large crowding down of charge carriers with a consequent large static field distortion. This leads to a smaller length L_n of the active region and a longer passive region (L_a). A decrease in the peak-to-valley ratio increases the length of the active region (L_n) and decreases the length of the passive region (L_a). This compensates for the reduced negative differential mobility until lower values of peak-to-valley ratio occur. Thus a significant increase in lattice temperature above room temperature is necessary to reduce the magnitude of the negative resistance by means of a change in the v-E curve.

3. Haddad, G. I. et al., "Microwave Solid-State Device and Circuit Studies," Tech. Report RADC-TR-71-109, Electron Physics Laboratory, The University of Michigan, Ann Arbor, June 1971.

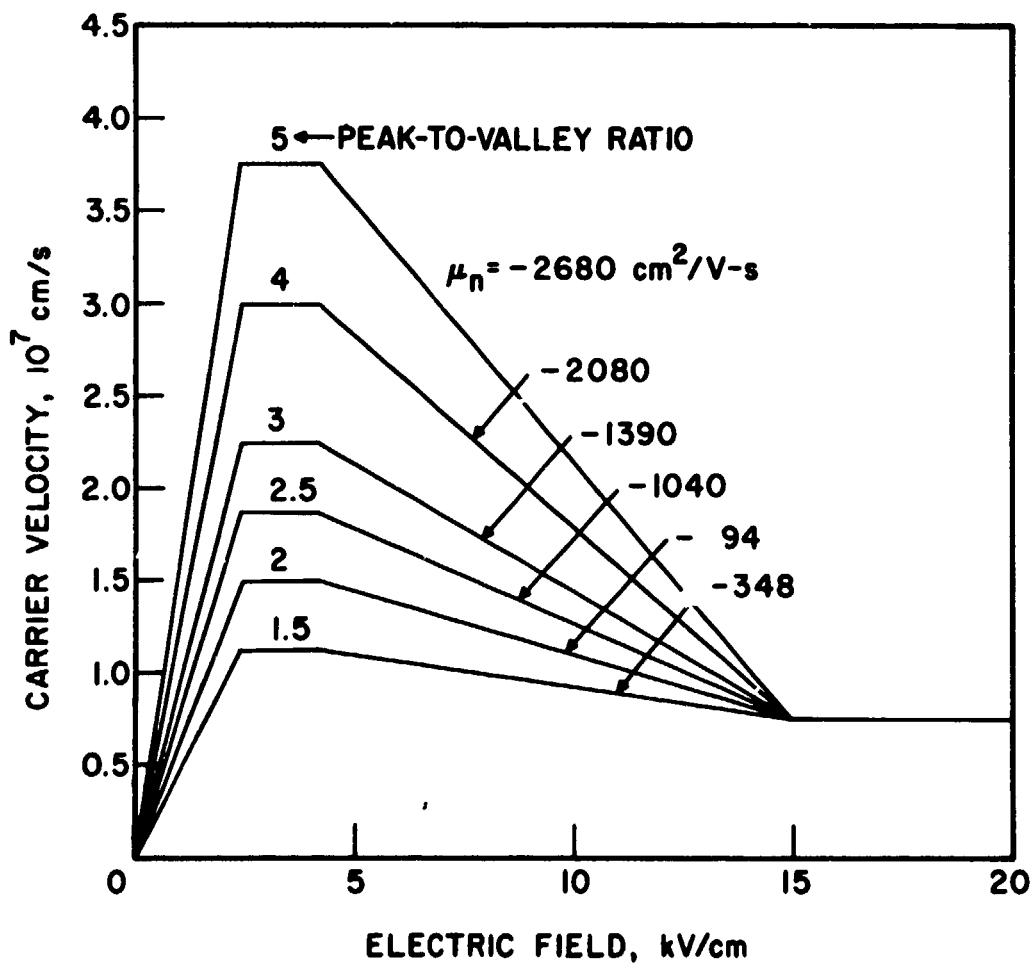


FIG. 3.4 VELOCITY-FIELD RELATIONSHIPS USED FOR SMALL-SIGNAL DIFFUSION-FREE STUDY.

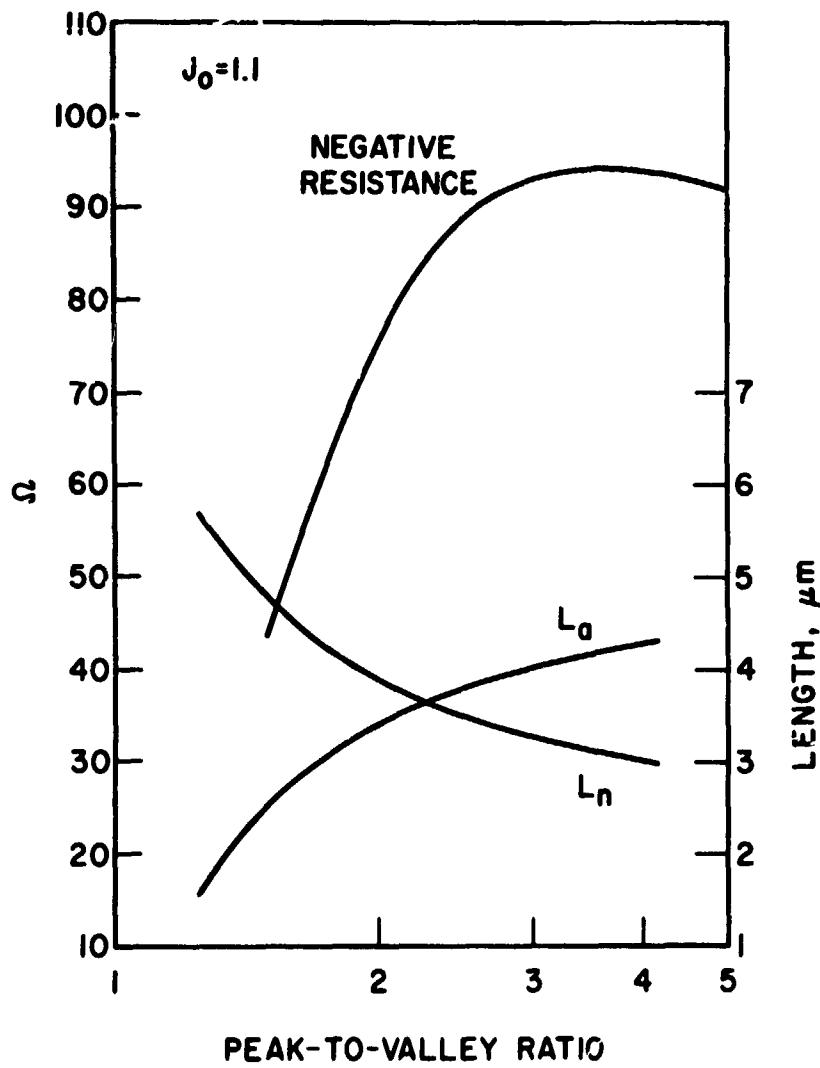


FIG. 3.5 DIFFUSION-FREE, SMALL-SIGNAL CALCULATIONS OF MAXIMUM NEGATIVE RESISTANCE AND LENGTH OF ACTIVE (L_n) AND PASSIVE (L_a) REGIONS IN A DEVICE $10 \mu\text{m}$ LONG WITH $n_o = 5 \times 10^{14}/\text{cm}^3$ AND AREA $= 7 \times 10^{-4} \text{ cm}^2$. VELOCITY-FIELD RELATIONS OF FIG. 3.4 WERE USED.

It was mentioned previously that static field distortion is high when the peak-to-valley ratio is large or at lower temperatures. To illustrate this effect, plots of static electric field vs. distance from the cathode are shown in Fig. 3.6 for $n_0 = 5 \times 10^{14}/\text{cm}^3$ and $J_0 = 1.1$. These were calculated by applying the large-signal analysis including diffusion effects, for the analytical forms of v-E characteristics, described in the last quarterly progress report for 300°K, 375°K and 500°K. These calculations are for a small-signal case.

The large-signal resistance and reactance were then calculated for the same material parameters and a bias of approximately 16 V: $l = 10.1 \mu\text{m}$, area = $7 \times 10^{-4} \text{ cm}^2$ and J_{11} , the normalized RF current, equals 0.15. These results are shown in Fig. 3.7. The bias voltage was kept constant by adjusting the value of J_0 for each temperature. The increase in temperature is seen to reduce the magnitude of maximum negative resistance and also the frequency at which it occurs. The major changes occur at this highest temperature, 500°K.

It was shown earlier³ that an increase in RF signal drive increases the static field distortion in the crystal leading to a greater voltage drop across the device for a constant dc current. In a constant voltage circuit, then, as the RF signal level increases, the increase in static field distortion will lead to a current drop in the bias current.

In addition to this current drop, Perlman et al.⁴ have observed that in CW devices additional current drop occurs at high bias voltages due to heating of the crystal. The present theory permits a calculation of this

4. Perlman, B. S., Upadhyayula, C. L. and Siekanowicz, W. W., "Microwave Properties and Application of Negative Conductance Transferred-Electron Devices," Proc. IEEE, vol. 59, No. 8, pp. 1229-1237, August 1971.

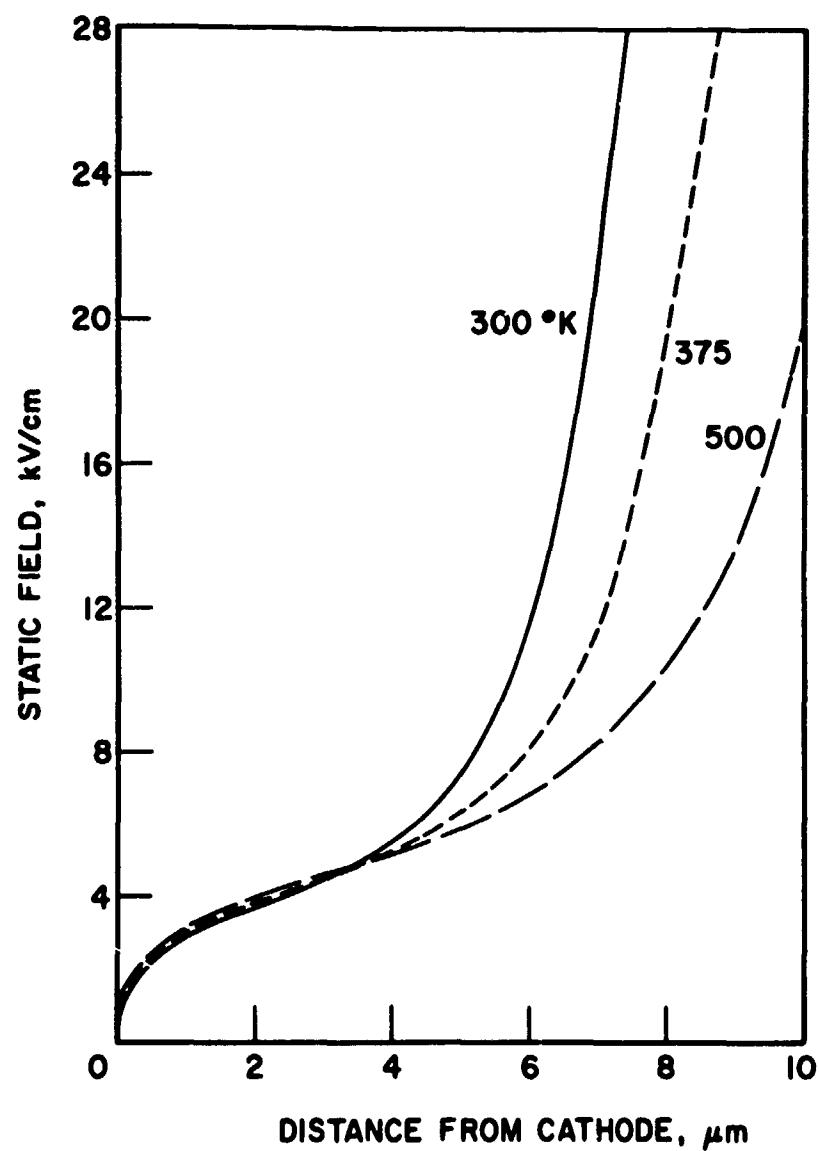


FIG. 3.6 STATIC ELECTRIC FIELD VS. DISTANCE FROM THE CATHODE FOR A SMALL-SIGNAL CASE AT DIFFERENT LATTICE TEMPERATURES WITH DIFFUSION EFFECTS INCLUDED. ($J_0 = 1.1$, $J_{11} = 0.001$, FREQUENCY = 10 GHz AND $n_0 = 5 \times 10^{14}/\text{cm}^3$)

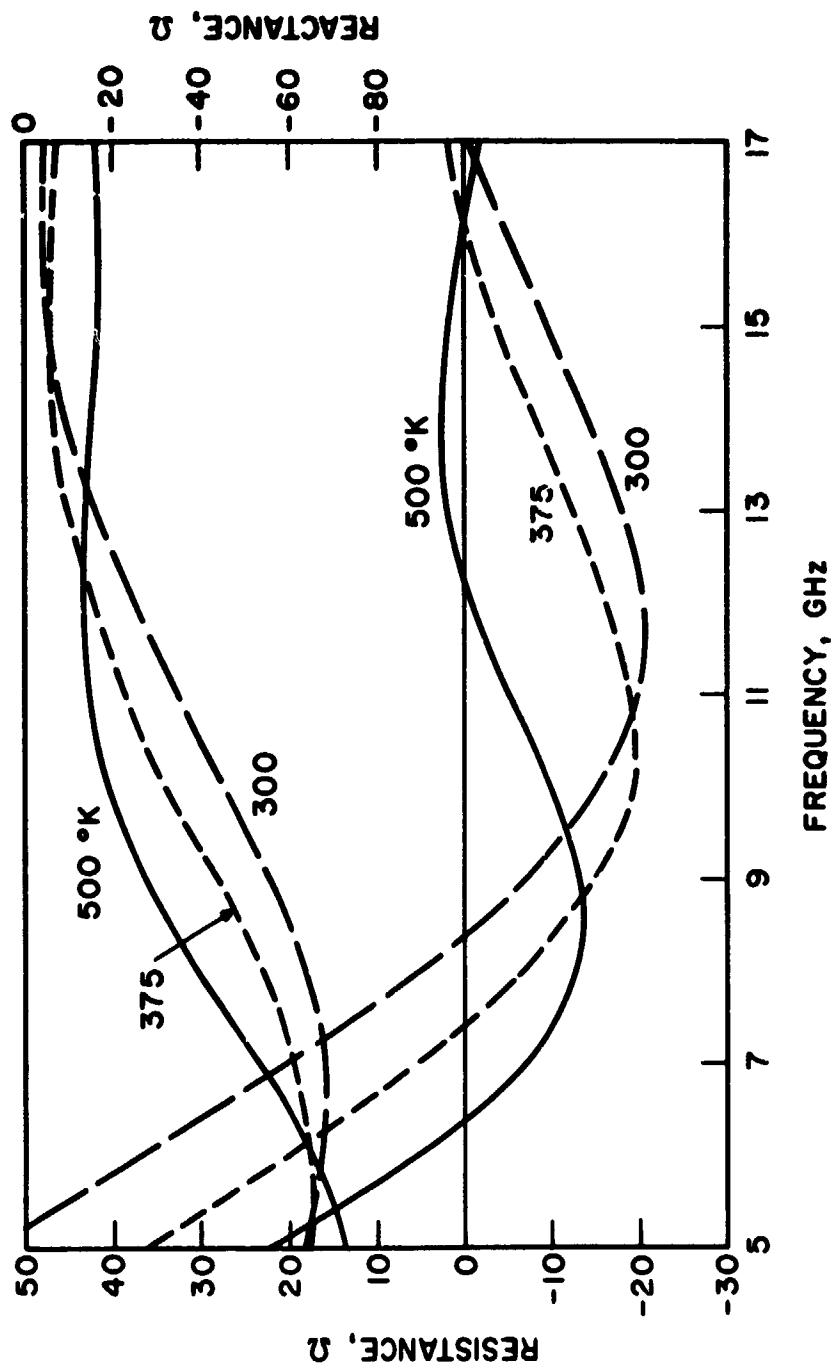


FIG. 3.7 IMPEDANCE VS. FREQUENCY AT DIFFERENT LATTICE TEMPERATURES WITH DIFFUSION EFFECTS INCLUDED. ($n_0 = 5 \times 10^{14} / \text{cm}^3$, BIAS VOLTAGE = 16 V, LENGTH = $10.1 \mu\text{m}$, AREA = $7 \times 10^{-4} \text{ cm}^2$ AND $J_{11} = 0.15$)

current drop and some results are shown in Fig. 3.8 where the device dc current is plotted as a function of bias voltage for small ac signals and a crystal length of 10 μm , $n_0 = 5 \times 10^{14}/\text{cm}^3$ and area = $3.5 \times 10^{-4} \text{ cm}^2$. The plot is in two parts. The section at low bias voltages is for a lattice temperature of 375°K and the one at higher bias voltages is for a lattice temperature of 500°K. If, in the CW operation, the bias is increased resulting in an increase in the lattice temperature from 375°K to 500°K, the operation of this device will move from some point on the 375°K curve to a point on the 500°K curve depending on the thermal resistance of the packaged device. If the device is initially operated at point A in the figure, then the bias is increased and the lattice temperature reaches 500°K. The operating points for four different values of the thermal resistance are shown in the figure. All show a current drop from point A. The higher the thermal resistance, the smaller is the bias voltage required to reach 500°K and the larger is the current drop.

3.5 Variation of the Lattice Temperature Along the Length of the GaAs Device. It was shown in the last quarterly progress report that an increase in static field distortion causes an increase in dc power dissipation and consequently a reduction in the dc to RF conversion efficiency of stabilized GaAs devices. The static field distortion occurs in GaAs because the average carrier velocity is smaller at high electric fields and since the electric field increases monotonically from cathode to anode, the charge carriers have a small average velocity near the anode compared to the point where the electric field is near threshold. This difference in velocity causes charge accumulation to occur near the anode in order to satisfy the condition of continuity of current. If the region

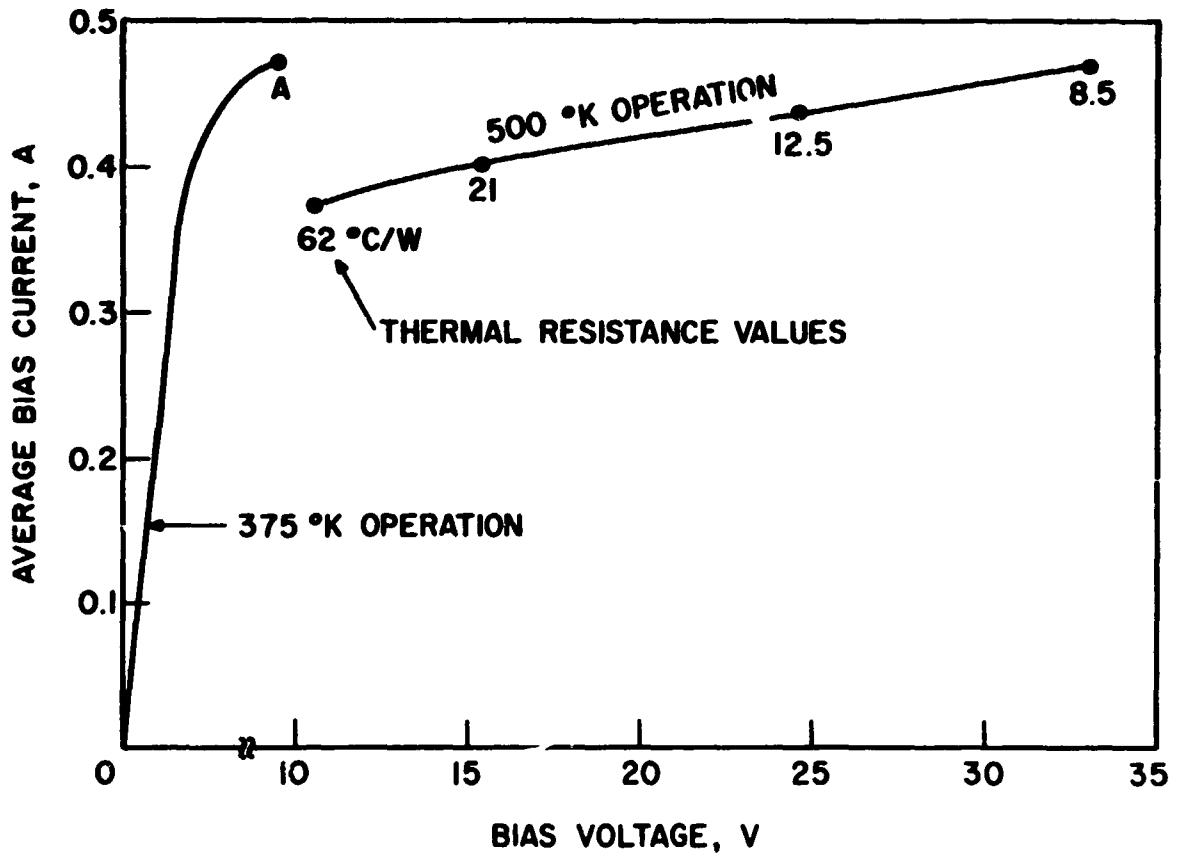


FIG. 3.8 Dc DEVICE CURRENT VS. BIAS VOLTAGE AT TWO DIFFERENT LATTICE TEMPERATURES. (LENGTH = 10 μ m, AREA = 3.5×10^{-4} cm^2 AND $n_o = 5 \times 10^{14}/\text{cm}^3$)

of the crystal near the anode were cooled to a lower temperature in comparison to the region near the cathode, the velocity of the charge carriers near the anode would be increased and this would lead to a reduced space-charge accumulation and consequently a smaller static field distortion. The same dc result can be obtained by heating the whole crystal, thereby reducing the peak-to-valley ratio. The situation is not the same however when RF behavior is considered. In the dc case the field varies only in space, whereas when RF is considered there is also a fluctuation of electric field with respect to time. Thus it is likely that different effects are obtained when there are lattice temperature gradients with temperature decreasing away from the cathode than when the whole crystal lattice is heated.

A study³ of the effects of lattice temperature can be made by assuming the parameters a_1 , a_2 and E_n of the velocity-field characteristics to be dependent on x , the distance from the cathode. Preliminary calculations have been made and it has been found that considerable improvement in the efficiency can be achieved if the lattice temperature decreases away from the cathode. The results will be reported in a future report.

3.6 Variation in Donor Density Along the Length of a GaAs Crystal.
It has been stated previously that the static field distortion results from an accumulation of charges near the anode, required by the negative differential mobility in GaAs. It was maintained in Section 3.5 that the accumulation can be reduced by creating a gradient in lattice temperature along the length of the device. Another way of reducing the accumulation of excess carriers would be to increase the donor density away from the cathode. It is thus suggested that efficiency should improve if the doping profile

of the GaAs crystal is properly controlled. In the analysis presented in the previous quarterly progress reports, the donor density n_o was assumed constant. If n_o is not constant, then the diffusion current density must be written as

$$J_d = -e \left(n_o + \frac{\epsilon}{e} \frac{\partial E}{\partial x} \right) \frac{\partial D}{\partial E} \frac{\partial E}{\partial x} - \epsilon D \frac{\partial^2 E}{\partial x^2} - e D \frac{\partial n_o}{\partial x} . \quad (3.2)$$

The last term is the new contribution. The solution of the problem with $\frac{\partial n_o}{\partial x} \neq 0$ can be carried out as done previously in Quarterly Progress Report No. 3.

3.7 Conclusions. Consideration of many numerical cases using the large-signal theory of stabilized TE devices permits the following conclusions to be drawn:

1. Stabilized TE devices show a fairly large bandwidth which appears to increase as the length of the crystal is reduced.
2. Inclusion of the field dependence of diffusion is important for accurate evaluation of dc quantities.
3. High operating temperatures are necessary for significant reduction of the magnitude of negative RF resistance which aids stabilization of the TE devices.
4. It is suggested that static field distortion in low n_o devices can be reduced by creating a lattice temperature gradient with temperature decreasing away from the cathode or by increasing the doping density near the anode.

3.8 Program for the Next Quarter. Theoretical calculations will be continued to study the effect of varying donor density in a stabilized

GaAs transferred-electron device. Experiments will be conducted to verify the salient results of the large-signal analysis. Experiments in the delayed-domain mode of operation will also be conducted.

4. Modulation Properties of Gunn-Effect Devices

Supervisor: W. R. Curtice

Staff: D. Tang

4.1 Introduction. The objective of the present study is to determine the effect of lattice temperature upon the frequency modulation sensitivity of Gunn-effect devices. The experimental results are presented and discussed in the following section.

In addition, the impedance of a waveguide mounting structure is investigated for the purpose of designing a cavity that has constant real loading over X-band frequency and a large tuning rate.

4.2 Experimental Investigation of Modulation Properties of a Gunn-Effect Device at Different Temperatures. Experiments at different temperatures were performed using the Gunn-effect device HB-10B-105 mounted in a 50Ω coaxial-line cavity. The cavity slugs are set so that resonant frequency of the cavity is about 8.6 GHz and the slugs are not removed throughout the experiments. The experimental setup is drawn schematically in Fig. 4.1.

The I-V characteristics are measured and plotted in Figs. 4.2 through 4.4 for heat sink temperatures of 8.5°C , -38°C and -61°C , respectively. The threshold current increases and low-field resistance decreases as temperature drops. This reflects the mobility increases when temperature drops because the electron carrier concentration is constant through the temperature range of the experiments. The large amount of dc current decrease at large bias

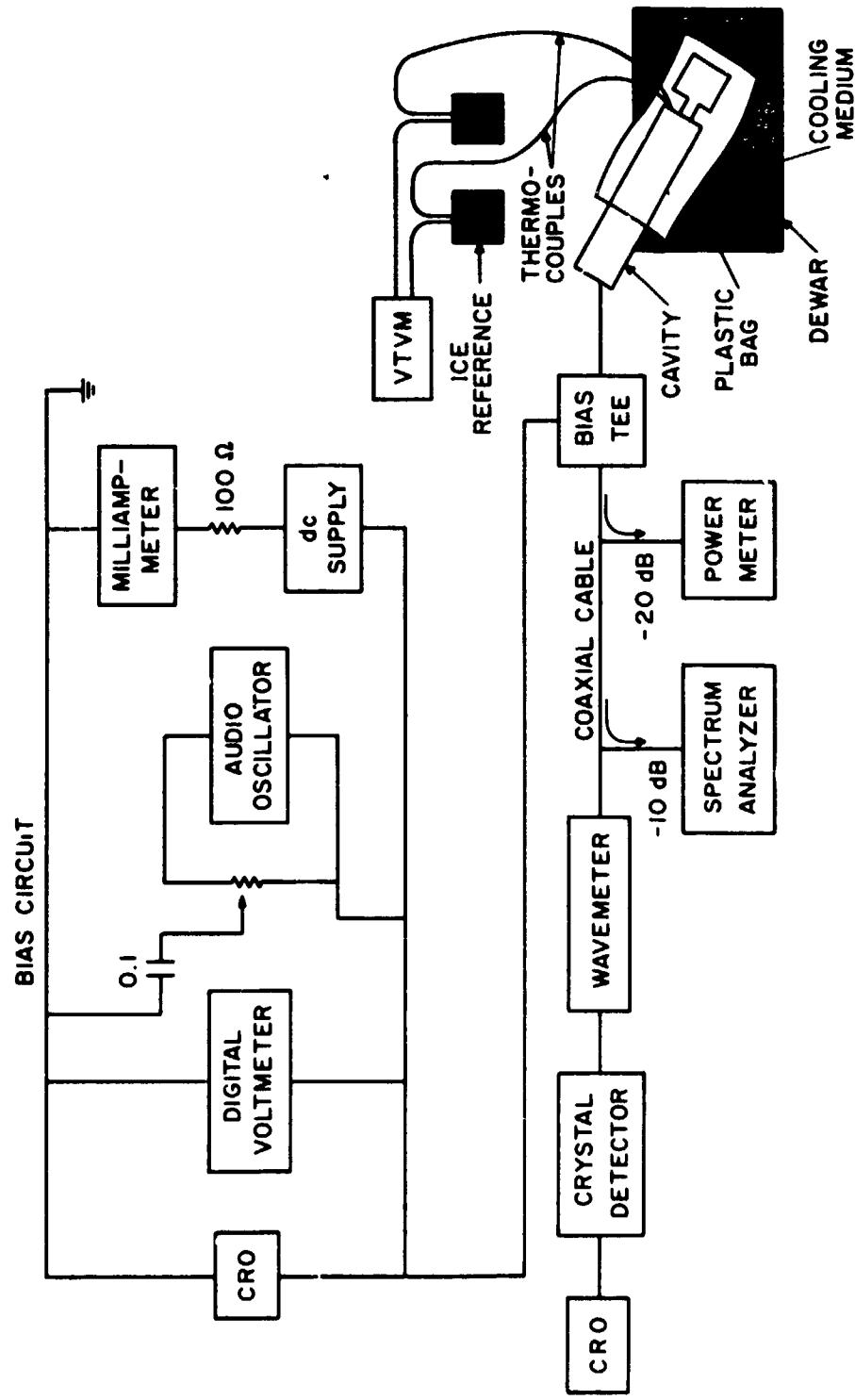


FIG. 4.1 EXPERIMENTAL SETUP.

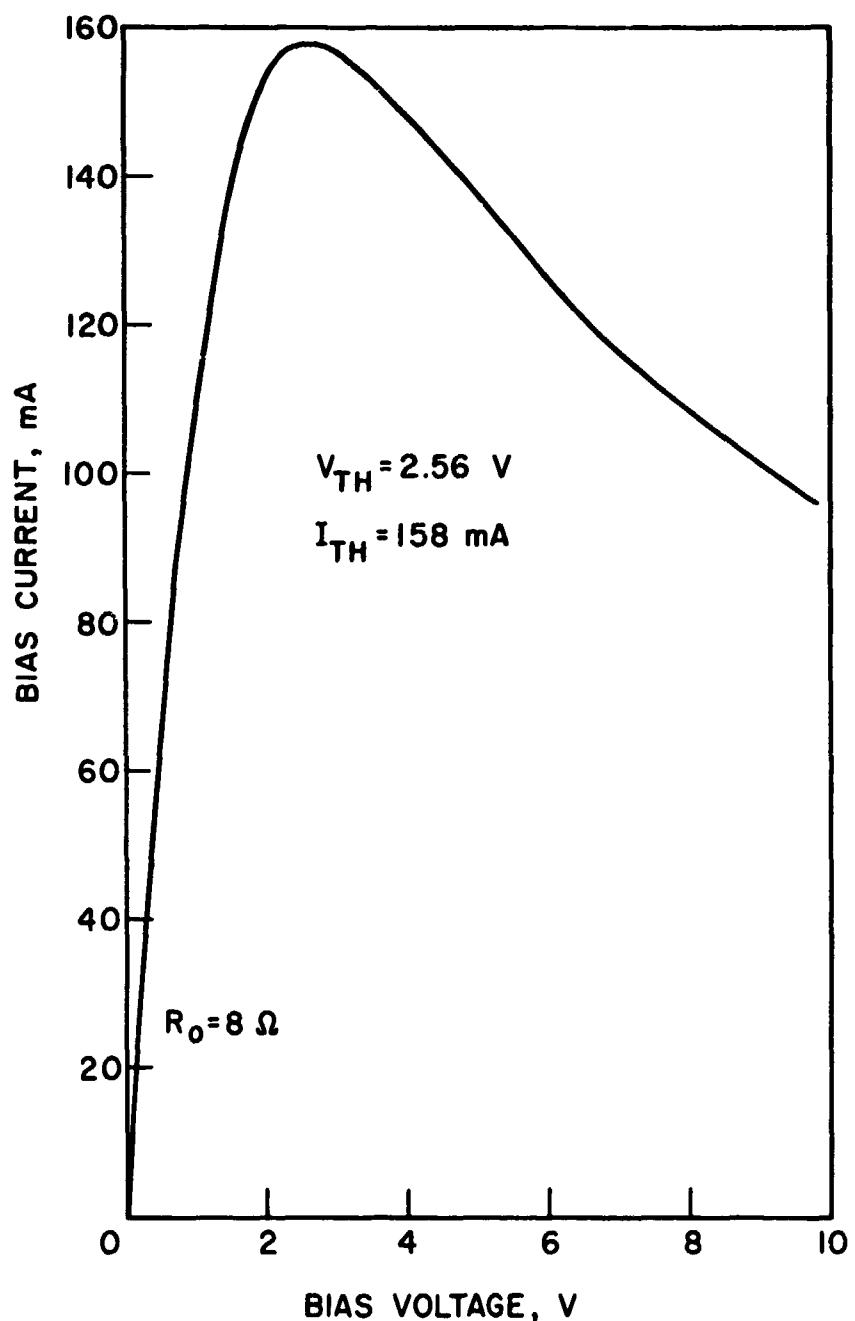


FIG. 4.2 I-V CHARACTERISTICS OF DEVICE HB-10B-105 FOR HEAT SINK TEMPERATURE
AT 8.5°C. THE LOW-FIELD RESISTANCE IS 8 Ω .

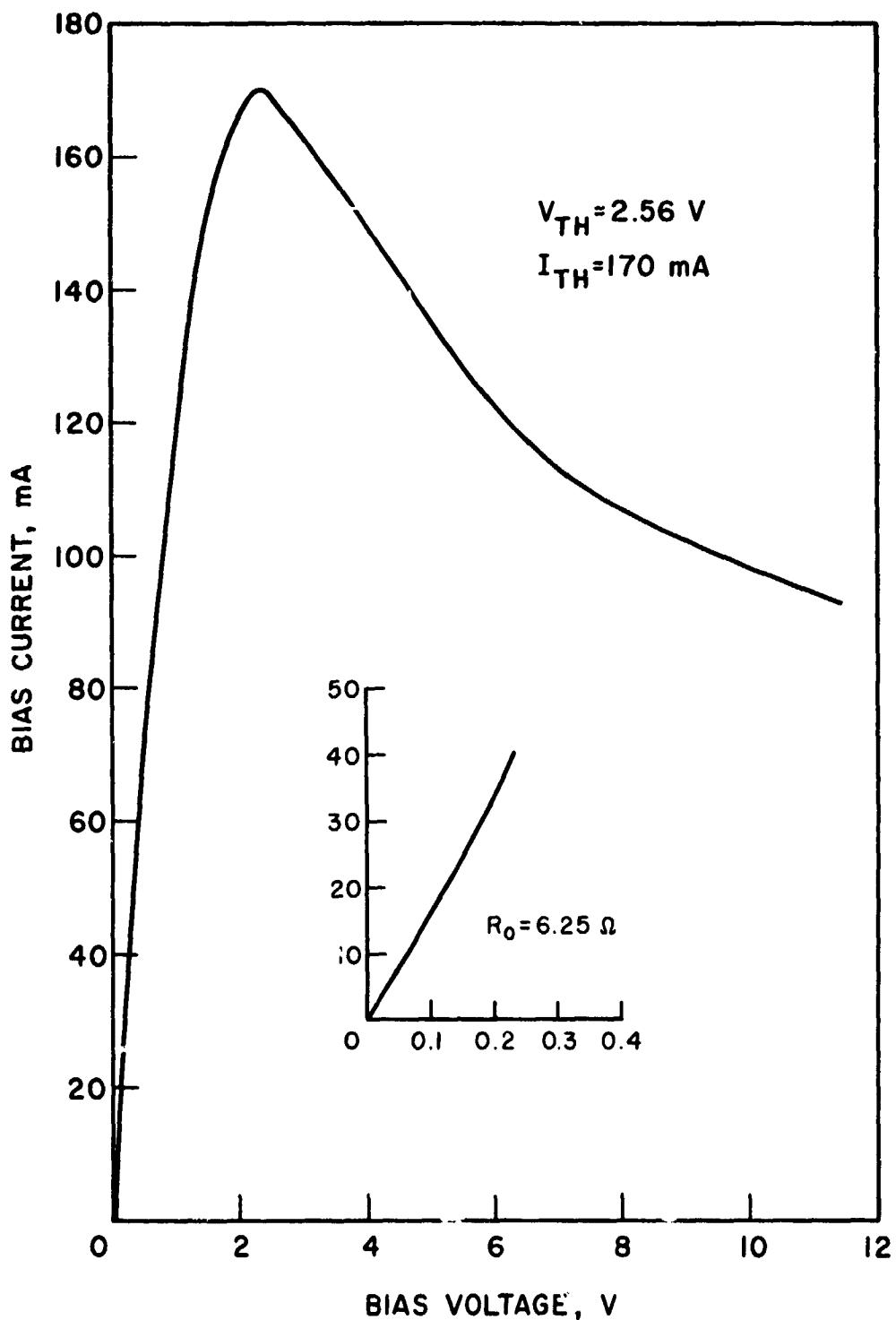


FIG. 1.3 I-V CHARACTERISTICS OF DEVICE HB-10B-105 FOR HEAT SINK TEMPERATURE AT -38°C . ENLARGED LOW-FIELD CHARACTERISTIC AND LOW-FIELD RESISTANCE ARE DRAWN UNDER THE CURVE.

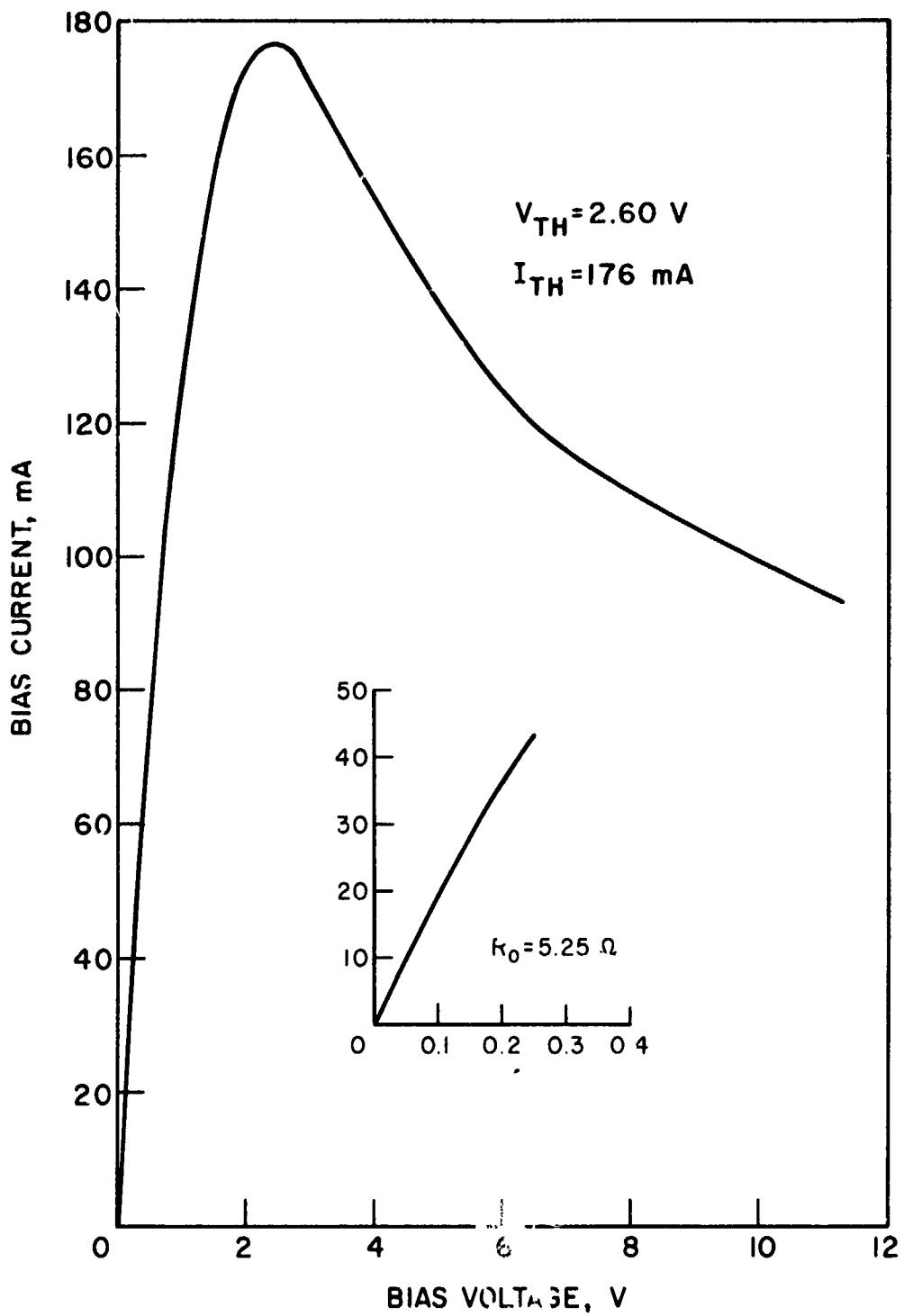


FIG. 4.4 I-V CHARACTERISTICS OF DEVICE HB-10B-105 FOR HEAT SINK TEMPERATURE AT -61°C. ENLARGED LOW-FIELD CHARACTERISTIC AND LOW-FIELD RESISTANCE ARE DRAWN UNDER THE CURVE.

voltage results from the device large thermal resistance. The device temperature increases rapidly with bias increase resulting in a rapid decrease in current with an increase in bias voltage. Device parameters are estimated to be as follows:

device length $\approx 10 \mu\text{m}$,

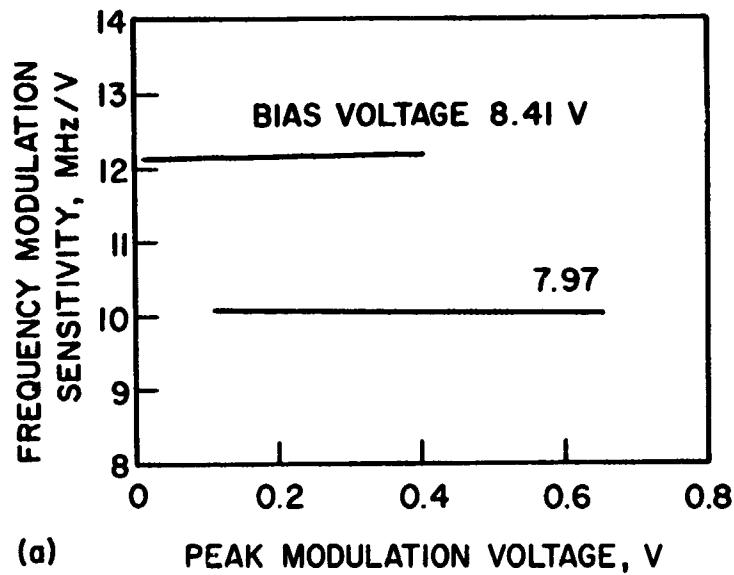
carrier concentrations 1 to $3 \times 10^{15} \text{ cm}^{-3}$,

Hall mobility at room temperature $\approx 8.2 \times 10^3 \text{ cm}^2/\text{V-s}$ and

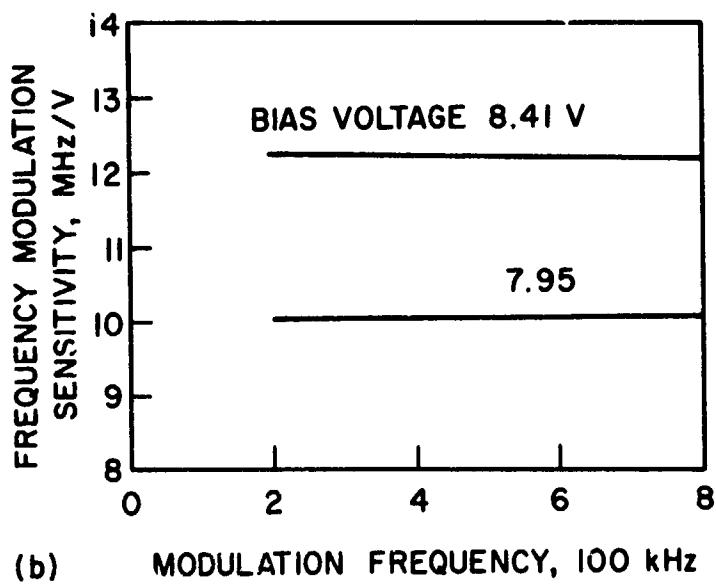
thermal resistance $\approx 260^\circ\text{C/W}$.

Data for frequency modulation sensitivity (FMS) is taken at different bias voltages for temperatures at 8.5°C , -21°C , -38°C and -61°C . The data show the FMS is constant over the modulation frequency range from 200 kHz to 800 kHz. It is also constant over the modulation voltage from 0 V to 1.5 V (peak value). Typical data are shown in Figs. 4.5a and 4.5b. The FMS varies rapidly with temperature and bias voltage. Its value varies from 1 MHz/V to 17.6 MHz/V. Figure 4.6 is a plot of FMS vs. bias voltage for different heat sink temperatures. Figure 4.7 is a plot of FMS vs. device average temperature by assuming thermal resistance of the device to be 260°C/W . Generally, FMS decreases when either temperature or bias voltage is increased.

Amplitude modulation sensitivity (AMS) is defined as the percentage power variation per unit modulation voltage (peak value). All the data show that AMS decreases as modulation frequency increases as shown in Figs. 4.8 and 4.9. The amplitude envelope of AM waveform is observed from the CRO. It is found that at low modulation frequency the waveform is more distorted than at high modulation frequency. This occurs because the device is nonlinear with respect to the modulation voltage. Higher



(a) PEAK MODULATION VOLTAGE, V



(b) MODULATION FREQUENCY, 100 kHz

FIG. 4.5 FREQUENCY MODULATION SENSITIVITY FOR HEAT SINK TEMPERATURE AT -38°C
(a) AS A FUNCTION OF PEAK MODULATION VOLTAGE AND (b) AS A FUNCTION
OF MODULATION FREQUENCY.

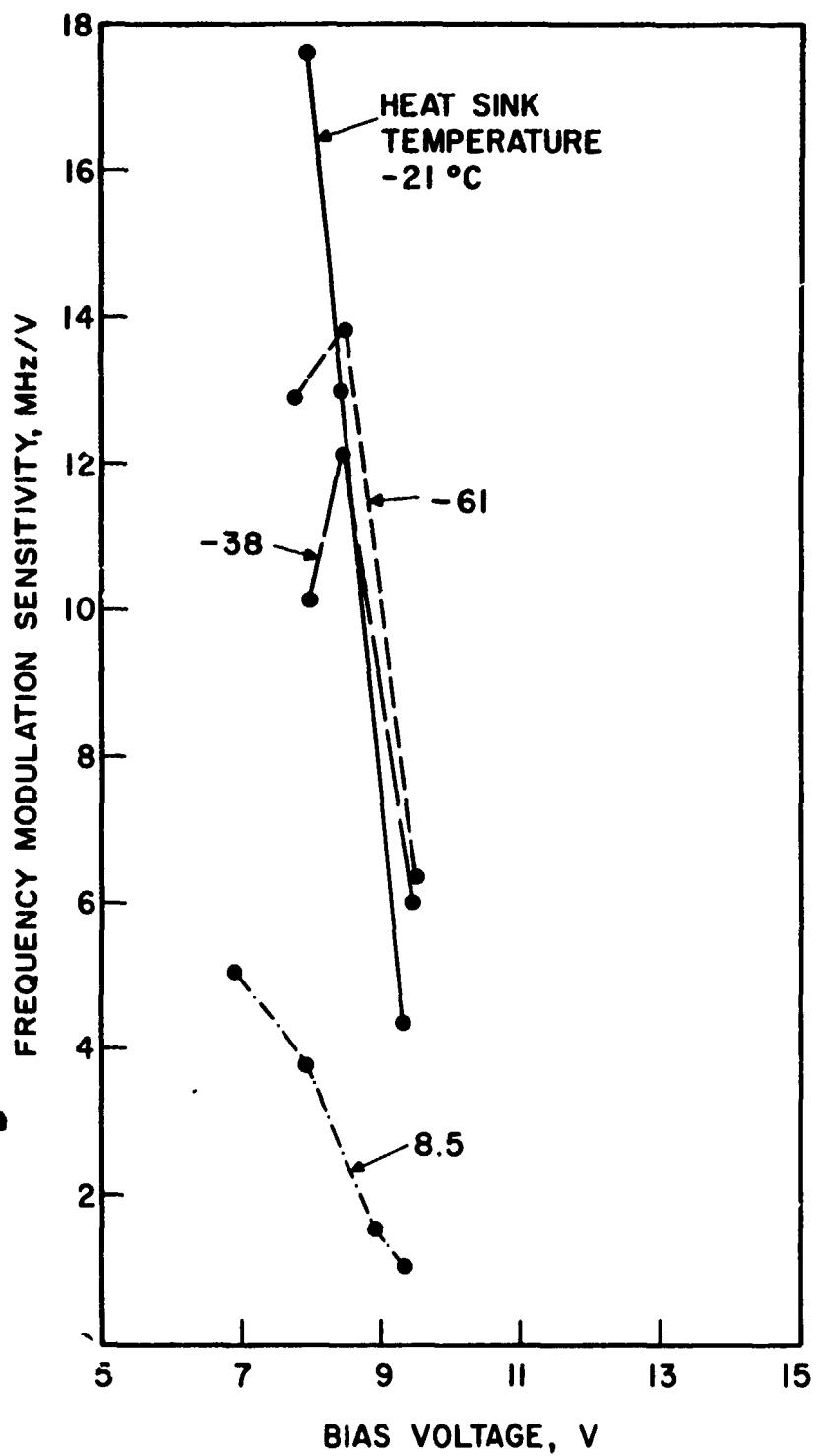


FIG. 4.6 FREQUENCY MODULATION SENSITIVITY VS. BIAS VOLTAGE FOR DIFFERENT HEAT SINK TEMPERATURES.

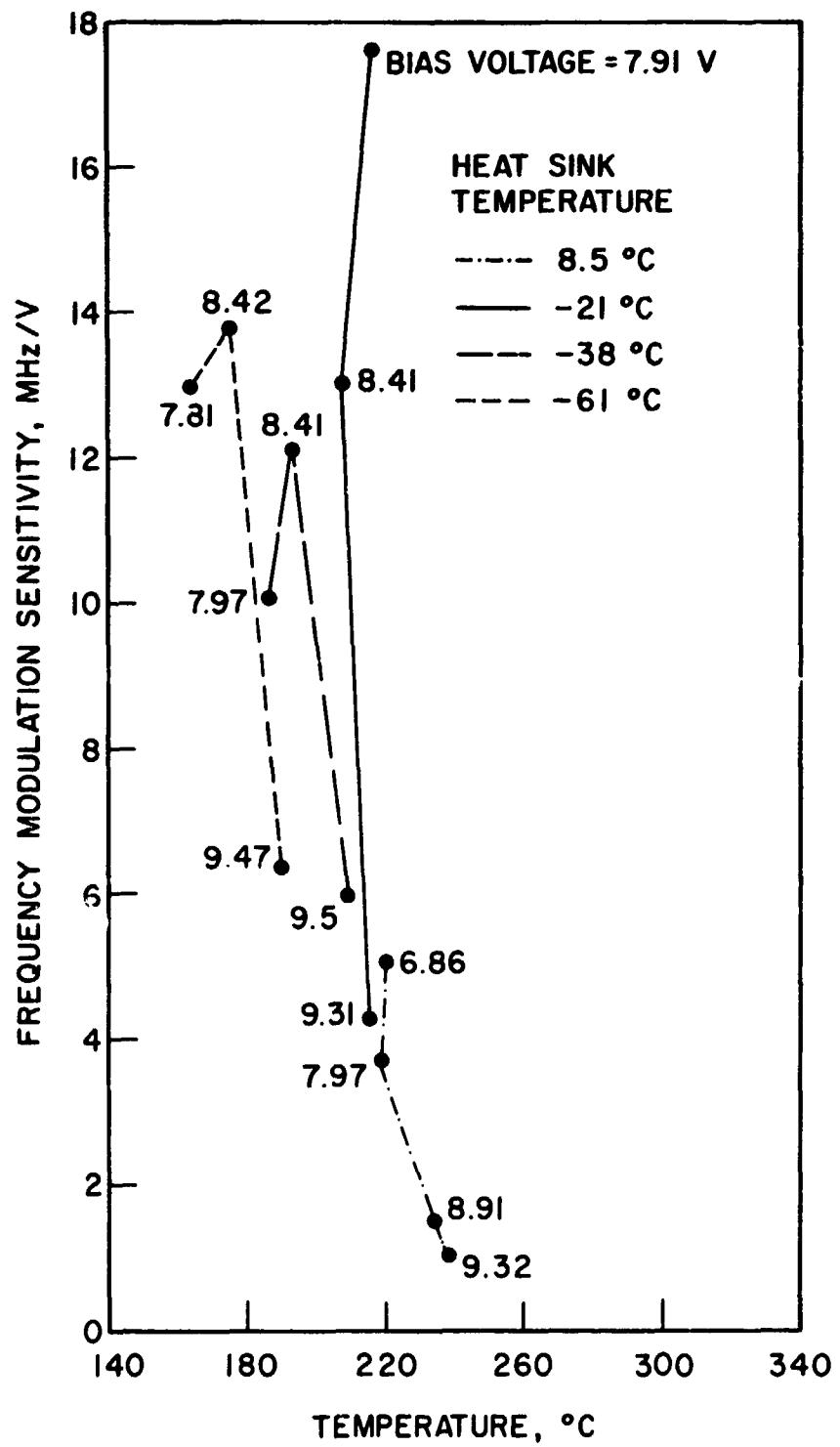


FIG. 4.7 FREQUENCY MODULATION SENSITIVITY VS. DEVICE AVERAGE TEMPERATURE.

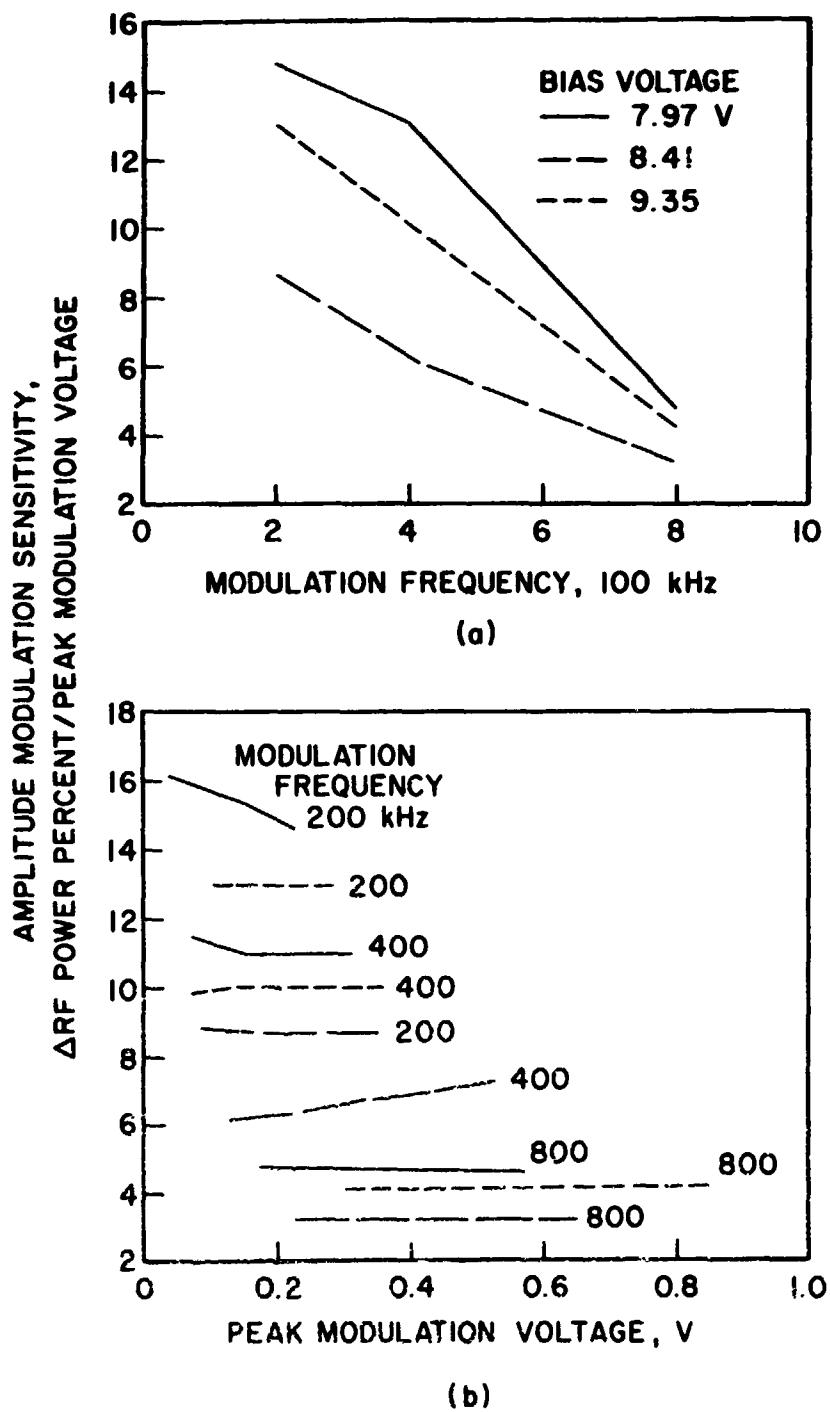


FIG. 4.8 AMPLITUDE MODULATION SENSITIVITY FOR HEAT SINK TEMPERATURE AT 8.5°C AND RF FREQUENCY AT 8.56 GHz. (a) AS A FUNCTION OF MODULATION FREQUENCY WHEN THE MODULATION VOLTAGE IS AT 0.2 V AND (b) AS A FUNCTION OF MODULATION VOLTAGE.

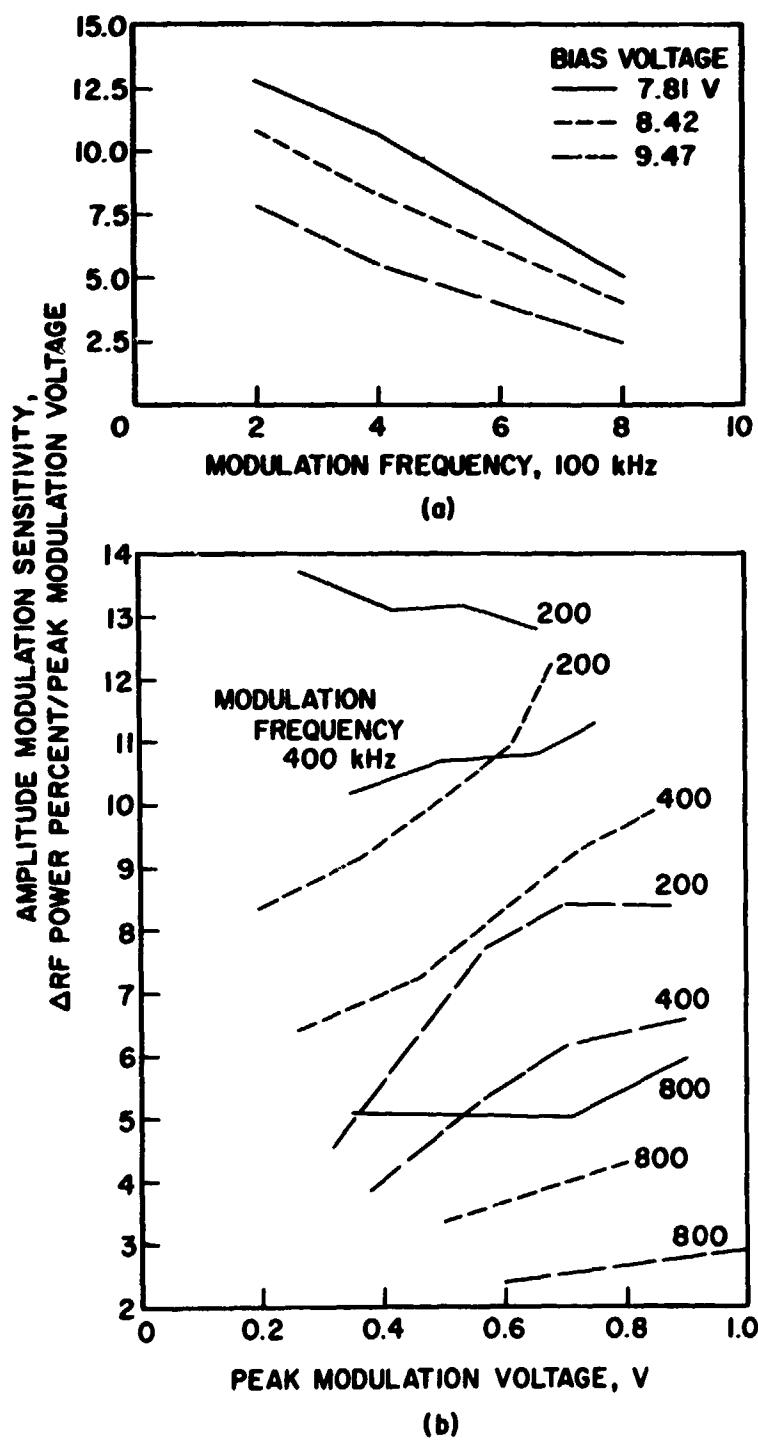


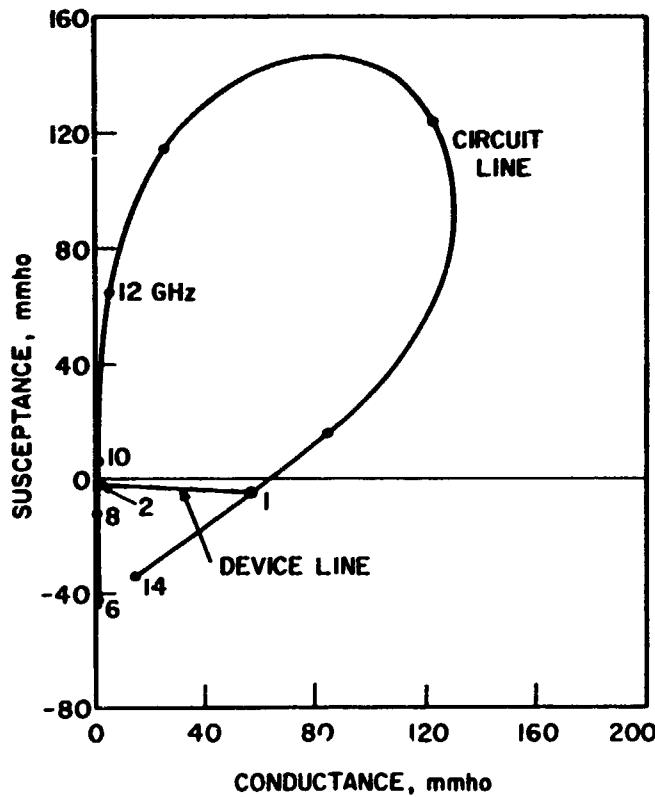
FIG. 4.9 AMPLITUDE MODULATION SENSITIVITY FOR HEAT SINK TEMPERATURE AT -61°C AND RF FREQUENCY = 8.68 GHz. (a) FOR PEAK MODULATION VOLTAGE AT 0.6 V AS A FUNCTION OF MODULATION FREQUENCY AND (b) AS A FUNCTION OF PEAK MODULATION VOLTAGE AT DIFFERENT BIAS VOLTAGES.

harmonics of the modulation frequency are produced by the device. The distortion is more apparent at low temperature.

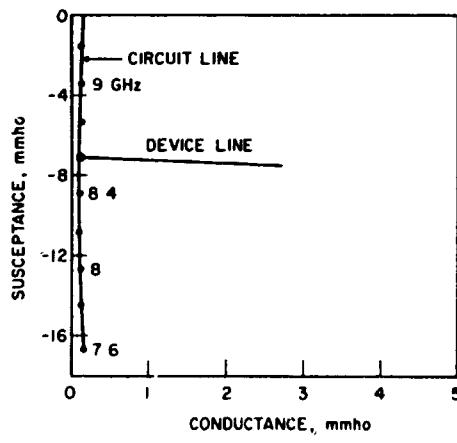
4.3 Device Operation in Waveguide and Coaxial Circuits. In this section the modulation sensitivities are discussed qualitatively. By plotting the cavity circuit admittance and the negative of device admittance on the complex admittance plane it can be seen how the circuit and the device affect the modulation sensitivities. The coaxial cavity and the waveguide cavity circuit have some similarities.

Figure 4.10a is a plot of the circuit line of the coaxial cavity used in the experiment and Fig. 4.11a is a typical X-band waveguide cavity circuit line. Both lines are computed including the package reactances. The scales on the circuit lines mark the corresponding frequency. The scale is wider at the right-hand part of the circuit line. The negative of the device line is also drawn in Figs. 4.10a and 4.11a. The stable oscillation point is the intersection of the device line and the circuit line at which the circuit line satisfies the condition $\partial B / \partial f > 0$. In Figs. 4.10a and 4.11a the points labeled 2 are the stable operating points. Figures 4.10b and 4.11b are the enlarged plot of the region near the operating point in Figs. 4.10a and 4.11a, respectively.

From the experimental data for the coaxial circuit it is found that increasing the bias voltage usually causes the frequency to increase. This reflects that the intersection point shifts upward along the circuit line. If the modulation frequency is not so high that the device admittance behaves as it does at steady state, it is found that the operating point traces up and down along a section of the circuit line. This is shown in Fig. 4.11b. The FMS is proportional to the frequency range of the circuit line covered

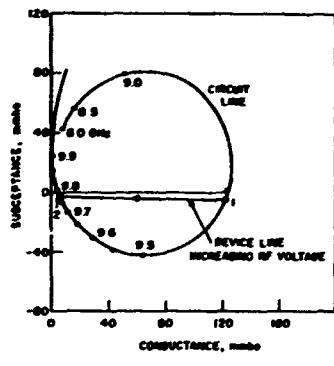


(a)

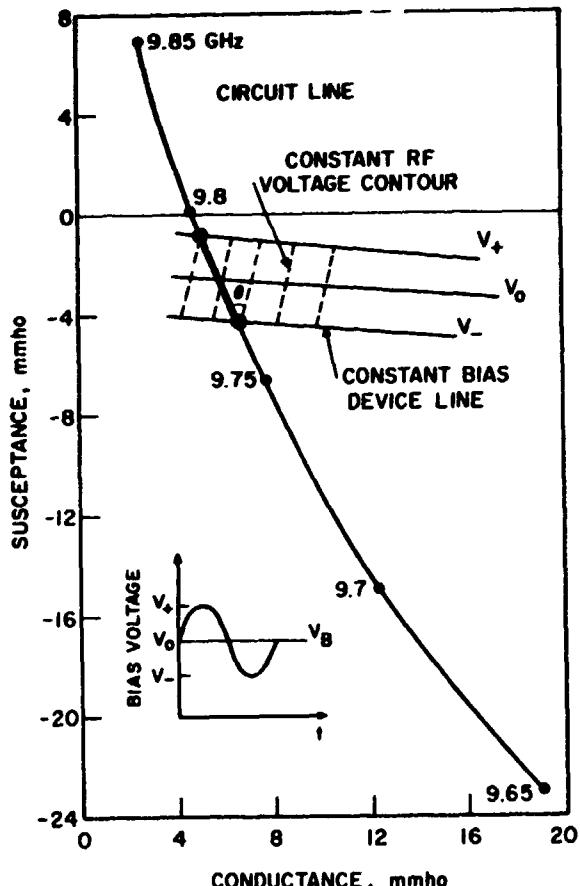


(b)

FIG. 4.10 (a) CALCULATED COAXIAL CAVITY CIRCUIT AND DEVICE LINES FOR THE EXPERIMENT AND (b) ENLARGED FIGURE NEAR POINT 2 IN FIG. 4.10a.



(a)



(b)

FIG. 4.11 (a) TYPICAL WAVEGUIDE CAVITY ADMITTANCE AND NEGATIVE DEVICE ADMITTANCE FOR A CONSTANT BIAS VOLTAGE AND (b) ENLARGED FIGURE NEAR POINT 2 IN FIG. 4.11(a) AND DEVICE LINES FOR DIFFERENT BIAS VOLTAGES.

by that section. The AMS is proportional to $\tan \theta$, where θ is the intersect angle between the constant RF voltage contour on the device lines and the circuit line.

Employing the preceding admittance plot, it can also be seen how the device temperature affects the modulation sensitivity. Raising the device temperature always decreases the oscillation frequency. This means the operating point shifts downward along the circuit line. If the scale is wider there, smaller FMS is expected.

Increasing bias voltage is usually accompanied by raising device temperature because the dc power dissipation increases. The resultant effect of increasing bias may shift the operating point either upward or downward depending on the thermal resistance of the device.

Device effects can be discussed by comparing the experimental data of FMS with the circuit line in Fig. 4.10b. Table 4.1 contains the data taken for heat sink temperature at -21°C . The RF frequency changes less than 70 MHz. In this frequency range, the frequency scale on the circuit line is almost uniform as shown in Fig. 4.10b. But the FMS changes nearly four times. It is apparent that the difference comes from the device itself.

Table 4.1
Gunn Device Behavior for Several Bias Voltages

<u>Bias Voltage (V)</u>	<u>FMS (MHz/V)</u>	<u>RF Frequency (GHz)</u>	<u>RF Power (mW)</u>
7.91	17.5	8.614	10.1
8.41	13.0	8.620	12.5
9.31	4.4	8.554	13.0

4.4 Waveguide Mounting of Devices. In a waveguide cavity the mounting post works as an antenna in the waveguide. RF power generated from the device is radiated through the post into the waveguide. The device driving point impedance is equal to the radiation impedance of the post. It is found that post reactance is directly proportional to the waveguide height and decreases with increasing post diameter.¹ For the post-gap structure which is used for mounting the device, only limited references are available. Eisenhart's theory² is applicable to the case where the gap is smaller than one fourth of the guide height (his post-gap reactance deviates from that given by Marcuvitz by 22Ω for the gap being one fourth of the guide height). When the device and its package are put into the gap, the strength and the distribution of the electric field in the gap are different from that of the air gap, and therefore the driving point impedance is different. The effect of the package and the device in the gap changes the gap capacitance. It is expected that if the package height, which is the gap height, is small compared with the guide height, then the reactance of the full height post is an approximation for the mounting post and the gap capacitance must be modified to be a larger value. Its exact numerical value depends on the package dimension.

In order to determine the circuit parameters which limit the R/Q ratio (or tuning rate) of half-wavelength-type waveguide cavity, calculations

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1. Marcuvitz, N., Waveguide Handbook, McGraw-Hill Book Co., Inc., New York, pp. 271-272, 1951.
 2. Eisenhart, R. L., "Theoretical and Experimental Analysis of a Waveguide Mounting Structure," Ph.D. Thesis, The University of Michigan, 1971.

were made with circuit parameters changed arbitrarily and the R/Q ratios were computed for each set of the parameters. It was found that neither the post inductance nor the gap capacitance limits the R/Q. The real loading and the package reactance do affect R/Q. The heavily loaded cavity (lower values of characteristic impedance Z_0) has a narrower frequency scale and therefore a larger tuning rate. For a reduced height X-band waveguide cavity with height-to-width ratio of 4.5, R/Q is 3.8Ω , while for a WR-90 waveguide cavity, R/Q is about unity. The tuning rate was computed for direct coupling of the package into a fully reduced height waveguide cavity which does not have a post in it, and the waveguide characteristic impedance was kept the same by reducing the width of the waveguide. The calculated R/Q was still about the same as that obtained from the full height waveguide post coupling cavity. Therefore the conclusion is reached that the tuning rate is mainly determined by the package parameters and the waveguide impedance.

4.5 Conclusions. Tests of a CW Gunn-effect device show that FMS is constant with respect to the modulation frequency and the modulation voltage. It increases as temperature and/or bias voltage decreases. However, AMS decreases as the modulation frequency increases. A distorted power waveform is observed at lower modulation frequency. The nonlinear relationship between AMS and the modulation voltage is more apparent at lower temperature as the harmonic modulation sidebands are produced.

Effect of bias voltage and temperature on the FMS and AMS can be interpreted as the shifting of the device operating point along the circuit line where the distance between the frequency scale and the circuit line slope are different. The experimental data show large FMS variations in a

small RF frequency range where the frequency scale of the circuit line is nearly uniform. This FMS variation comes from the device itself.

When the package is postmounted in a waveguide cavity, the post inductance is nearly the same as a full height post in a waveguide. Neither the post inductance nor the gap (mounting) capacitance limits the R/Q ratio of a waveguide cavity. The waveguide characteristic impedance and the package parameters limit the R/Q ratio. A reduced height cavity heavily loads the device and improves the R/Q ratio.

4.6 Program for the Next Quarter. The investigation of modulation properties of Gunn-effect devices will be continued. Further tests of the temperature effects and bias voltage effects will be made for the waveguide mounting structure; mechanical tuning saturation will be studied. A cavity design with separately controllable external Q and tuning rate R/Q will be sought.

5. Avalanche-Diode Amplifiers

Supervisor: G. I. Haddad

Staff: R. W. Laton

5.1 Introduction. The objective of this phase of the program is to study the stability, large-signal gain bandwidth and saturation properties of avalanche-diode amplifiers and the dependence of these properties upon doping profile, biasing and circuit configuration.

During this reporting period a computer-aided synthesis procedure was developed for the determination of the equivalent circuit characterizing any particular diode package and mount configuration. Results were obtained utilizing this procedure for both microstrip and ridged waveguide mounts.

Wafer admittance characteristics were refined using the Read model program described¹ previously, but with more realistic avalanche region widths as determined by Schroeder and Haddad² for both Si and GaAs diodes. Terminal plane immittance plots were obtained using the transformation determined for the packaged diode terminating a 50- Ω microstrip line, and this information was used to begin the design of a microstrip reflection amplifier circuit.

5.2 Determination of Immittance Transformations Characterizing a Diode Package and Mount. In the previous quarterly progress report a computer program was described which perturbs assumed equivalent circuit element values in such a manner that the mean-square error between measured and calculated terminal impedance values is minimized. During this reporting period a systematic method of determining the configuration and starting values for the assumed elements has been developed, based upon classical methods for the synthesis of a lossless driving point impedance from the location of its poles and zeros.³

Begin by measuring the impedance as a function of frequency at the desired reference plane with the diode biased just below breakdown.

Figure 5.1 is a plot of such data for the case of a diode in a Type 023 package terminating a 0.650-inch length of 50- Ω microstrip line on a 0.25-inch thick alumina ($\epsilon_r \approx 10$) substrate. From this figure a lossy pole of

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1. Schroeder, W. E. and Haddad, G. I., "Effect of Harmonic and Subharmonic Signals on Avalanche-Diode Oscillator Performance," IEEE Trans. on Microwave Theory and Techniques (Correspondence), vol. MTT-18, No. 6, pp. 327-331, June 1970.
 2. Schroeder, W. E. and Haddad, G. I., "Avalanche Region Width in Various Structures of IMPATT Diodes," Proc. IEEE (Correspondence), vol. 59, No. 8, pp. 1245-1248, August 1971.
 3. Guillemin, E. A., Synthesis of Passive Networks, John Wiley and Sons, Inc., New York, Chap. 3, 1957.

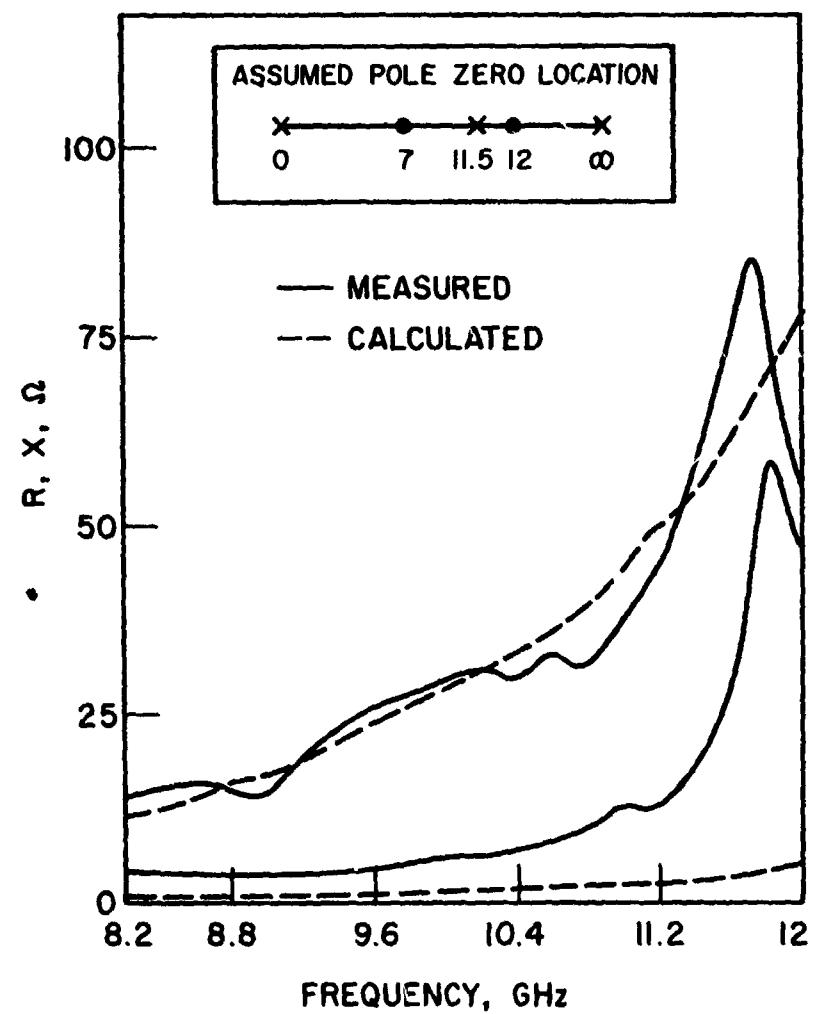


FIG. 5.1 MEASURED IMPEDANCE FOR A DIODE IN AN 023 PACKAGE TERMINATING A 50- Ω MICROSTRIP LINE. INSET SHOWS POSTULATED POLE-ZERO CHARACTERIZATION.

impedance is clearly evident at approximately 11.5 GHz. A passive lossless circuit must have poles and zeros which alternate along the $j\omega$ axis. Thus the simplest realization of the behavior shown in Fig. 5.1 is obtained from an impedance function containing a zero at the origin, a pole at 11.5 GHz and a zero at infinity. In fact, however, additional data at frequencies above and below those plotted in Fig. 5.1 indicate a change in sign of the reactance at frequencies immediately below 7.5 GHz, indicating a reactance zero at that frequency as well as a reactance which again increases with frequency from 12 to 12.4 GHz. The pole-zero configuration is postulated as shown at the top of Fig. 5.1. The impedance function may then be constructed as

$$Z(s) = H \frac{(s^2 + \omega_{01}^2)(s^2 + \omega_{03}^2)}{s(s^2 + \omega_{p2}^2)} , \quad (5.1)$$

where the impedance level factor H is chosen to match reactances at some desired $s_i = j\omega_i$ near the center of the frequency range of interest. Expansion of Eq. 5.1 into a ladder of two series of inductances and two shunt capacitances is straightforward. The final shunt capacitance should be as large or larger than the independently measured junction capacitance. If it is not, the impedance level of the final loop of the ladder network may be adjusted, for example, by multiplying the appropriate row and column of the impedance matrix by a constant. Finally, a small resistance is assumed in series with the junction capacitance to represent any undepleted substrate and ohmic contact losses. One ohm is a reasonable value. The end result, which forms the starting point for the optimization algorithm by the computer, is then shown in Fig. 5.2. Note that the parallel combination of

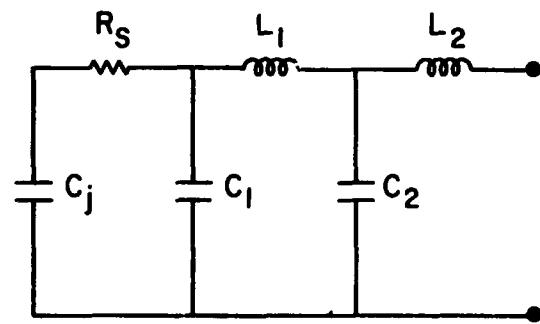


FIG. 5.2 ASSUMED EQUIVALENT CIRCUIT.

C_1 and C_j is equal to the capacitance value obtained for the final element in the ladder reduction of Fig. 5.1. Starting and final element values are shown in Table 5.1 and the calculated real and reactive parts are shown by the dashed lines in Fig. 5.1.

Table 5.1
Equivalent Circuit Element Values

<u>Element</u>	<u>Assumed Starting Value</u>	<u>Final Value</u>
R_S	1.5 Ω	1.5 Ω
C_1	0.188 pF	0.2203 pF
L_2	0.602 nH	0.553 nH
C_2	0.692 pF	0.4924 pF
L_3	0.283 nH	0.3016 nH
C_j (measured)	0.35 pF	0.35 pF

Several sources of inaccuracy must be commented upon. First, in the microstrip media with $\epsilon_r \approx 10$, the wavelength is decreased to approximately 40 percent of its free-space value. Therefore at 10 GHz $\lambda_{\text{microstrip}}$ is approximately 0.480 inch. The outer diameter of the diode package ceramic is 0.085 inch, which is about two thirds of a quarter-wavelength. Therefore, attempts to model the transformation with frequency-independent lumped elements can only be expected to be successful over fairly narrow ranges of frequency. Second, the impedance was measured using slotted-line techniques with an open circuit at the physical location of the edge of the diode package ceramic for a reference. The VSWR's obtained using the open circuit were rather low, particularly above 11 GHz, being of the order of 7 to 10. This means that the microstrip line itself was quite lossy in that frequency

range. The magnitude of the real part, as well as the reactive part, near the pole at 11.5 GHz is very strongly influenced by this loss, and both parts can be duplicated very closely from 11 to 12 GHz by allowing the series loss to go as high as 10Ω . The usefulness of a circuit with such a high loss is doubtful, therefore the circuit element values in Table 5.1 are regarded as a good approximation to the measured impedances from 8 to 11 GHz, even though they produce a pole (of much higher impedance) at a frequency of 13.5 GHz instead of 11.5 GHz.

5.3 Package Transformation in a Ridged Waveguide. The techniques described in Section 5.2 have been applied to the case of a diode in an 023 package mounted in ridged waveguide. The measured and calculated impedances are shown in Fig. 5.3 with the guide dimensions shown in the inset. The equivalent circuit is shown in Fig. 5.4. Since the diode is mounted in a transmission configuration with the far end of the guide terminated in a matched load, the 50Ω parallel resistance across the package terminals presents Z_0 , the characteristic impedance of the guide at approximately 9 GHz. Since all the loss could be placed in a single R_S or R_P , an ambiguity is introduced into the optimization scheme by the choice shown, with an attendant loss of effectiveness in minimizing real part error. Nevertheless, the result is considered good and both losses are retained in the interest of duplicating the physical situation. Finally, all the impedances are taken with a plane transverse to the axial dimension of the guide through the center line of the diode as a reference.

5.4 Admittance Characteristics of Si and GaAs Diodes. Recent work by Schroeder and Haddad² indicates significant differences in avalanche region width in complementary Si diodes because of the differing ionization

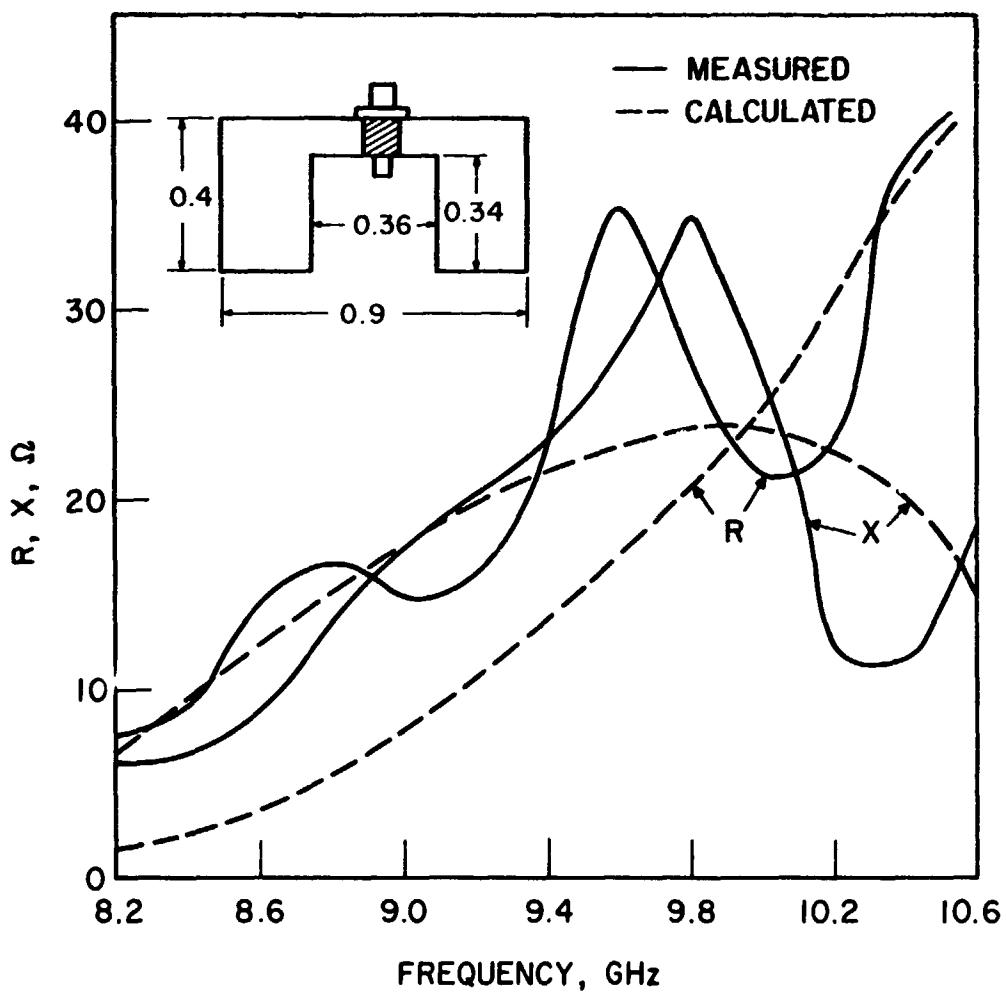
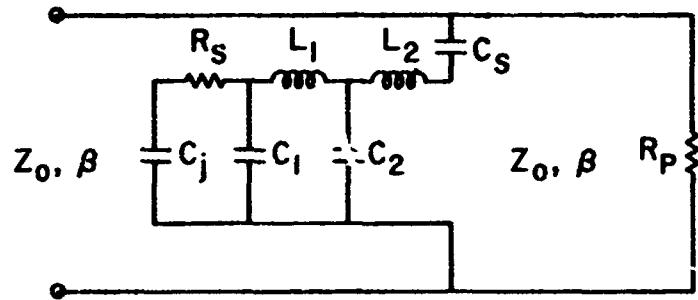


FIG. 5.3 MEASURED AND CALCULATED IMPEDANCES FOR A DIODE IN AN 023 PACKAGE MOUNTED IN RIDGED WAVEGUIDE.



<u>Element</u>	<u>Value</u>
R_S	1 Ω
R_P [= $Z_0(f)$]	50 Ω
L_1	0.585 nH
L_2	0.84 nH
C_1	0.24 pF
C_2	0.94 pF
C_S	0.57 pF
C_j	0.35 pF

FIG. 5.4 EQUIVALENT CIRCUIT FOR A TYPE 023 PACKAGE IN RIDGED WAVEGUIDE.

rates for holes and electrons. Their results indicate an avalanche region width of approximately 40 percent in the commonly utilized p^+nn^+ Si diodes. Since our earlier theoretical work was based on admittance characteristics obtained assuming a 20 percent avalanche width, refinement of those curves was desirable. This was accomplished utilizing the Read model computer program for an avalanche width of $2.7 \mu\text{m}$ and a drift length of $4 \mu\text{m}$. For comparison, data were also obtained for a GaAs diode with an avalanche width of $1 \mu\text{m}$ and a drift length of $3 \mu\text{m}$. The bias current density was 1000 A/cm^2 in both cases, while the Si diode area was made larger so that equal reactances were obtained at the peak value of small-signal negative conductance. The results are shown in Fig. 5.5.

Since the GaAs diode clearly provides larger values of negative conductance, its characteristics were transformed through the equivalent circuit of Fig. 5.2 to provide a basis for design of a microstrip reflection amplifier. The transformed characteristics, on an impedance basis, are shown in Fig. 5.6.

5.5 Program for the Next Quarter. The design and fabrication of a microstrip reflection amplifier will be completed and experimental measurements undertaken during the next period. In addition, theoretical methods of loading and combining two transmission stages of amplification in ridged waveguide will be investigated.

6. High-Efficiency Avalanche Diodes

Supervisors: R. J. Lomax and G. I. Haddad

Staff: C. M. Lee

6.1 Introduction. The objectives of this phase of the program are to investigate numerically and experimentally avalanche diodes with a view

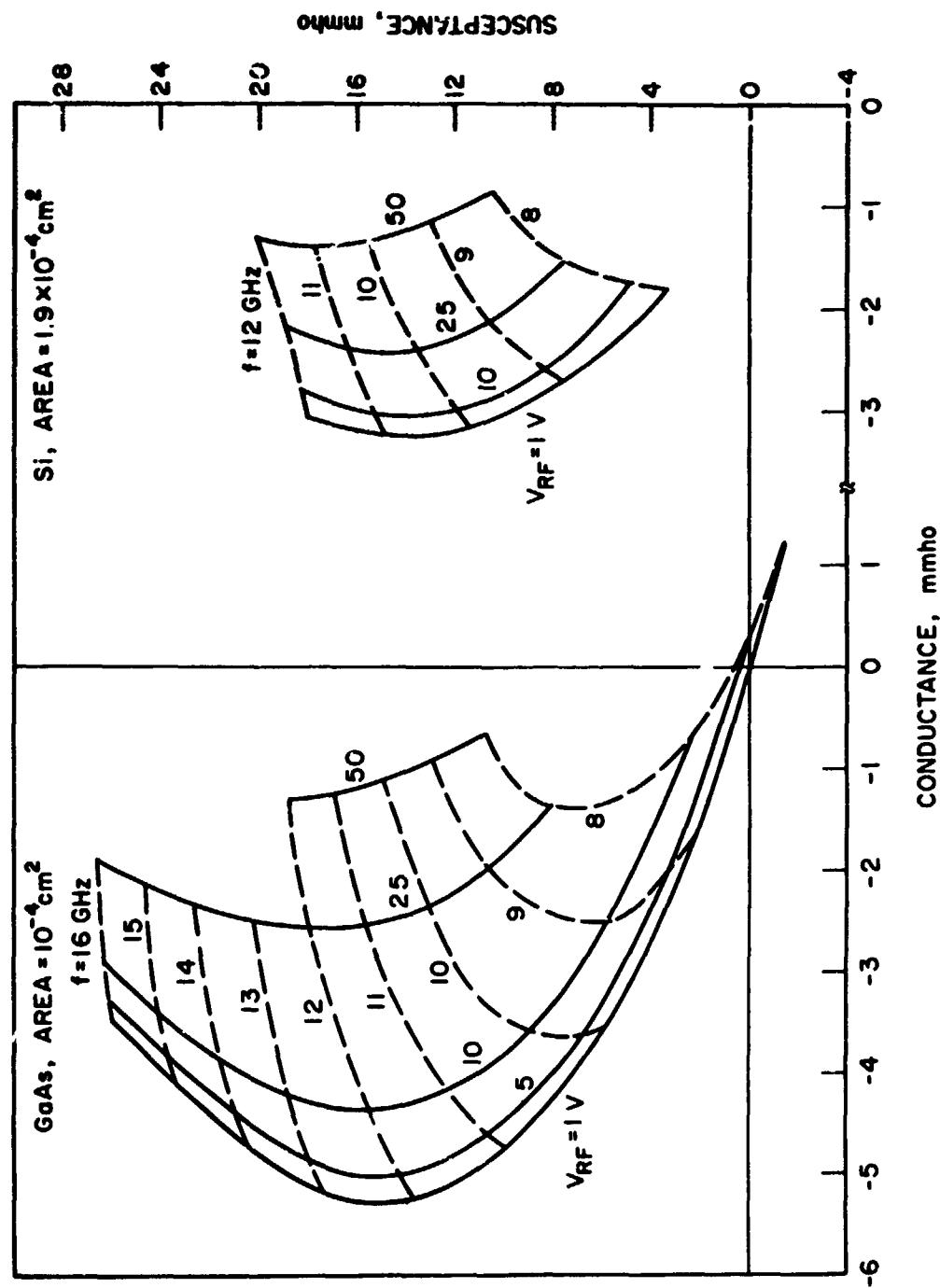


FIG. 5.5 COMPARISON OF ADMITTANCE CHARACTERISTICS FOR UNPACKAGED GaAs AND Si DIODES BIASED AT 1000 A/cm^2 .

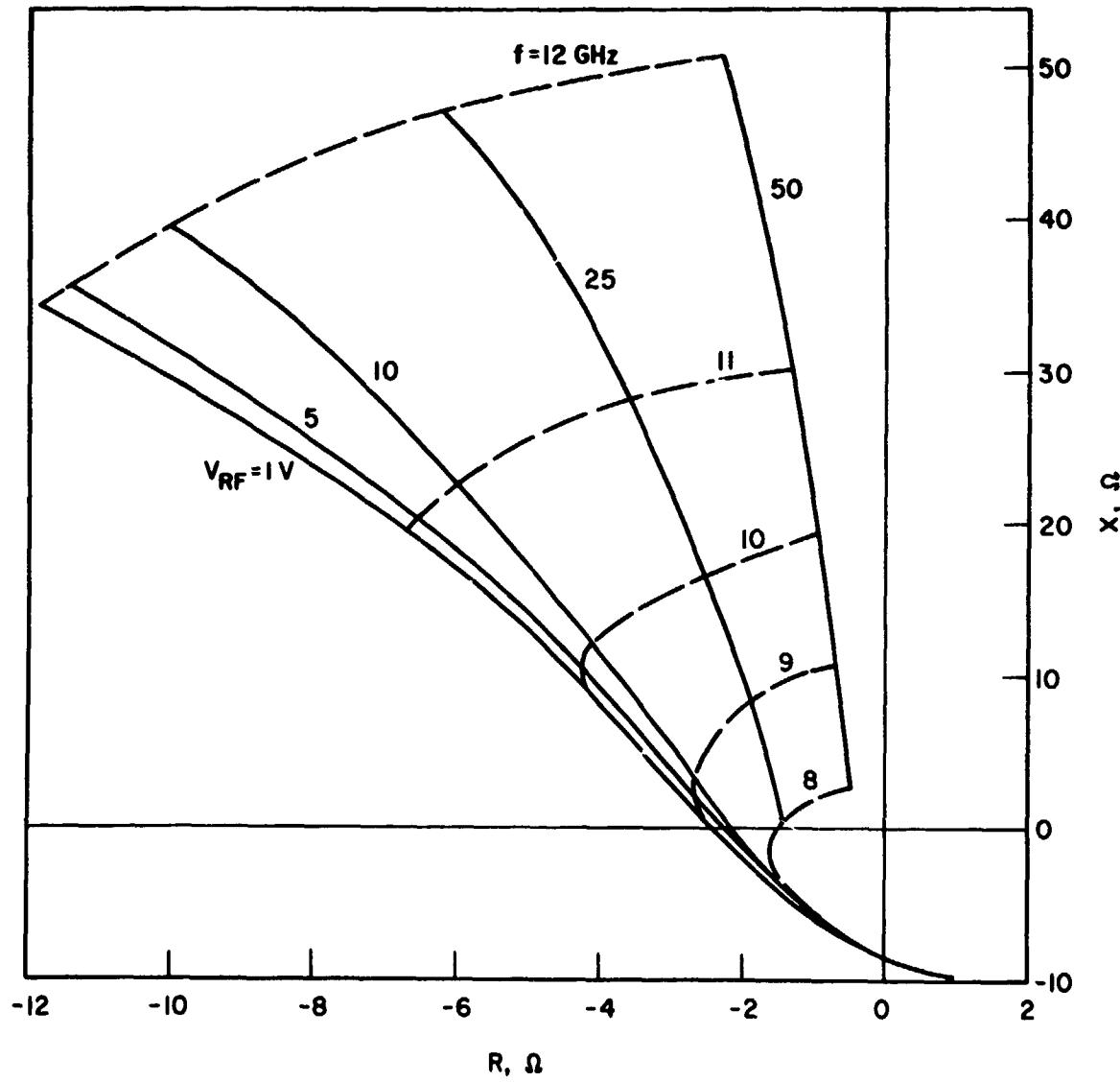


FIG. 5.6 TERMINAL IMPEDANCE FOR A PACKAGED (TYPE 023) GaAs DIODE IN A 50- Ω MICROSTRIP LINE AS A FUNCTION OF RF VOLTAGE ON THE WAFER AND FREQUENCY. ($J_o = 1000$ A/cm 2)

to devising techniques to increase the power output and efficiency of avalanche-diode oscillators and amplifiers. The aim of the numerical investigation is to develop a mathematical model which handles distributed avalanche, nonsaturated drift velocities and unequal ionization rates for electrons and holes, and then to use this mathematical model to investigate the operation of avalanche diodes of various constructions under various operating conditions. The aim of the experimental investigation is to test the validity of the theoretical results.

6.2 IMPATT Mode Computer Program. This computer program has been successfully developed, evaluated and used extensively in the investigation of the performance of complementary diodes. Its operation has been explained in detail in Quarterly Progress Report No. 3. It can handle distributed avalanche and unequal ionization rates for electrons and holes, however it requires that the drift velocities of carriers remain saturated. During this quarter, the effect of mesh size on the calculated admittance has been investigated. Figure 6.1 is a sample of the many curves obtained in this investigation which shows the convergence of the solution as the mesh size becomes smaller and smaller. These curves will help to determine the mesh size required for a given accuracy. Also during this quarter the method of calculating the admittance has been changed to accelerate the convergence. Previously, the total current was computed from the following equation

$$J_T = \epsilon \frac{\partial E}{\partial t} + q \cdot V \cdot (P + N) , \quad (6.1)$$

then the admittance was obtained by Fourier analyzing the J_T . Since Eq. 6.1 involves a numerical differentiation (namely, $\partial E / \partial t$) which always

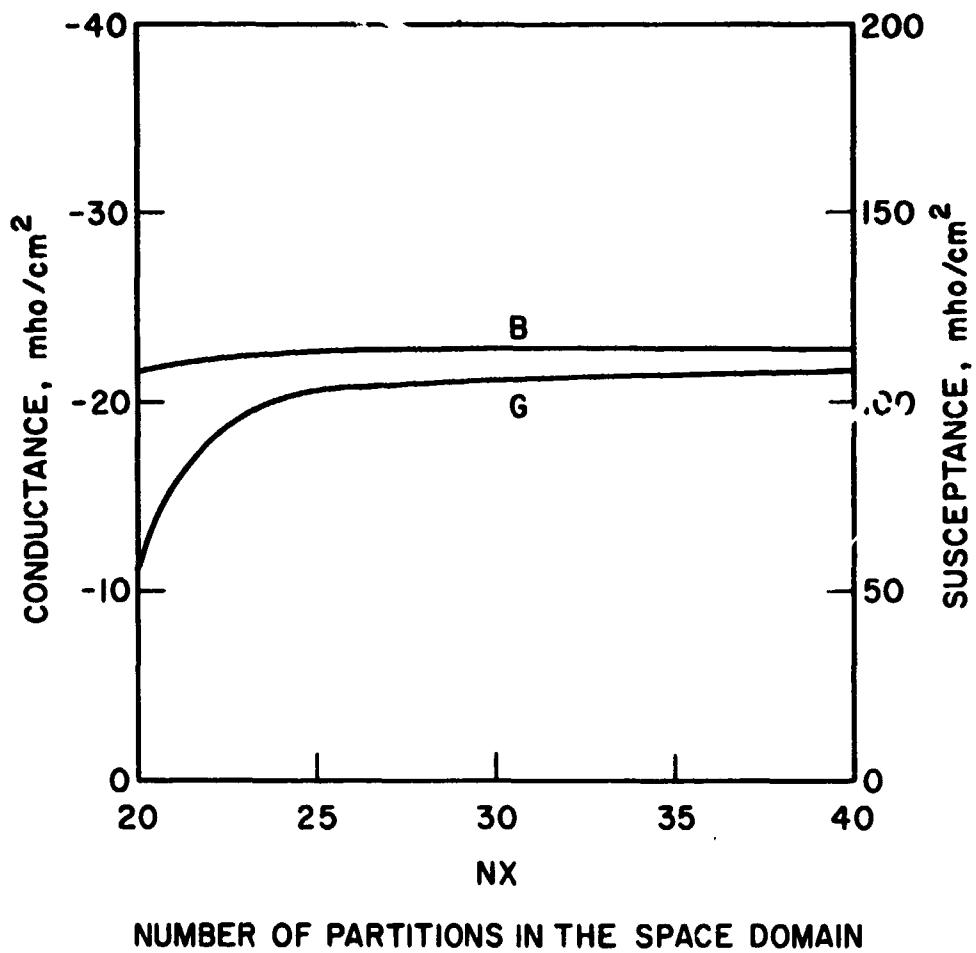


FIG. 6.1 EFFECT OF MESH SIZE.

amplifies errors in E , the calculated J_T tended to have large errors. Furthermore, because the conductance G usually has about one-tenth the magnitude of the admittance Y , the relative error in G was about ten times larger than that in Y or in J_T . All these effects tended to make the convergence rate slow. In the new method the total current J_T is separated into two components: the displacement current J_d and the induced current J_i . The displacement current J_d is due to the depletion layer capacitance, hence its associated admittance is the pure susceptance jB_d which can be calculated from

$$jB_d = j\omega C = j\omega\epsilon/W . \quad (6.2)$$

The induced current J_i is the space average of the space-charge current:

$$J_i = \frac{1}{W} \int_0^W (P + N) \cdot V \cdot dx . \quad (6.3)$$

Its associated conductance G_i and susceptance B_i can be found by Fourier analyzing $J_i(t)$. Since Eq. 6.2 does not have any finite difference error and Eq. 6.3 involves only numerical integration, the calculated conductance ($G = G_i$) and susceptance ($B = B_d + B_i$) are much less affected by numerical errors.

As a partial check for this program and for general use (e.g., see Section 7), a computer program has been written to calculate the small-signal admittance of an avalanche diode of arbitrary doping profile. This has the advantage of being inexpensive to run and to some extent the calculation is self-checking.

6.3 TRAPATT Mode Program. During TRAPATT mode operation the electric field in the avalanche diode may become very small or even negative, hence the assumption of saturated drift velocities made in the IMPATT mode program is no longer valid. Previously, the carrier currents were calculated first from the following equations:

$$JP(x, t) = JP_{sat} + \int_0^x \left(G - \frac{\partial P}{\partial t} \right) \cdot dx \quad (6.4)$$

and

$$JN(x, t) = JN_{sat} + \int_x^W \left(G - \frac{\partial N}{\partial t} \right) \cdot dx . \quad (6.5)$$

Next the carrier densities were calculated from

$$P(x, t) = JP(x, t)/VP \quad (6.6)$$

and

$$N(x, t) = JN(x, t)/VN . \quad (6.7)$$

Difficulties arise when the velocities become zero and Eqs. 6.6 and 6.7 become undefined. One way to avoid these difficulties is to introduce a diffusion term. Hence to consider variable velocities it is helpful to consider diffusion at the same time, and the continuity equations become:

$$-D \frac{\partial^2 P}{\partial x^2} + V_p \frac{\partial P}{\partial x} + P \frac{\partial V_p}{\partial x} + \frac{\partial P}{\partial t} = G \quad (6.8)$$

and

$$-D \frac{\partial^2 N}{\partial x^2} - V_n \frac{\partial N}{\partial x} - N \frac{\partial V_n}{\partial x} + \frac{\partial N}{\partial t} = G . \quad (6.9)$$

An iterative method is used to solve Eqs. 6.8, 6.9 and Poisson's equation. A FORTRAN program that will implement this method is currently being written.

6.4 Conclusions. The IMPATT mode computer program has been well checked out and used extensively, however, its application is limited to the IMPATT mode case in which the electric field does not usually fall below the saturation field. Development of the TRAPATT mode program which will handle variable velocities is being carried out.

6.5 Program for the Next Quarter. The development of the TRAPATT program will be continued. Once a correct mathematical model is achieved, systematic theoretical and experimental investigations will be carried out to optimize power output and efficiency.

7. Nonlinear Operating Characteristics of IMPATT Diodes

Supervisor: G. I. Haddad

Staff: W. E. Schroeder

7.1 Introduction. In the last quarterly progress report a large-signal IMPATT diode analysis which utilizes the concept of separable ionization and drift regions was described. During this reporting period extensive numerical results were obtained from the computer program. Several cases of interest are described.

7.2 Nonpunch-Through Silicon Diode. Consider the case of an $n^{+}pp^{+}$ diode where the doping level and width of the p-region are such that the region is not entirely depleted when the diode is reverse biased into breakdown. In the undepleted epitaxial region the electric field is low and the current flow is essentially ohmic. This situation is frequently modeled as a resistance in series with the impedance of the active, i.e., depleted region of the diode. This approach is simple and relatively accurate for small RF drive levels; however for large drive levels the depletion width is modulated and the field in the undepleted region may

exceed that required for constant mobility, thus complicating the picture. An alternative approach is to consider the entire p-region to be the active region and to find the current by solving the carrier transport equations throughout the region.

Using the IMPATT diode analysis described in the last quarterly progress report an X-band Si n^+pp^+ diode which breaks down prior to punch through was modeled. The p-region was taken to be uniformly doped at $5 \times 10^{15} \text{ cm}^{-3}$ with a total width of 9 μm , composed of a 1- μm avalanche region and an 8- μm "drift" region. The ionization rates of electrons and holes were taken equal to a single effective rate which is appropriate to Si at room temperatures:

$$\alpha_{\text{eff}} = A \exp\left(-\frac{b}{E}\right), \quad (7.1)$$

where $A = 1.315 \times 10^7 \text{ cm}^{-1}$ and $b = 2.46 \times 10^7 \text{ V/cm}$. The expression for drift velocity as a function of electric field is of the form given by Scharfetter and Gummel:¹

$$v(E) = \frac{k_1}{\left(\frac{k_2}{E^2} + \frac{1}{k_3 E + k_4} + k_5\right)^{1/2}}. \quad (7.2)$$

Values of the coefficients k_i which are appropriate for holes in room temperature Si were used. The resulting $v(E)$ has a low-field mobility of $480 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and a saturated velocity of $1.2 \times 10^7 \text{ cm/s}$; the complete function is plotted in Fig. 7.1. The diffusion coefficient was taken to be

1. Scharfetter, D. L. and Gummel, H. K., "Large-Signal Analysis of a Silicon Read Diode Oscillator," IEEE Trans. on Electron Devices, vol. ED-16, No. 1, pp. 64-77, January 1969.

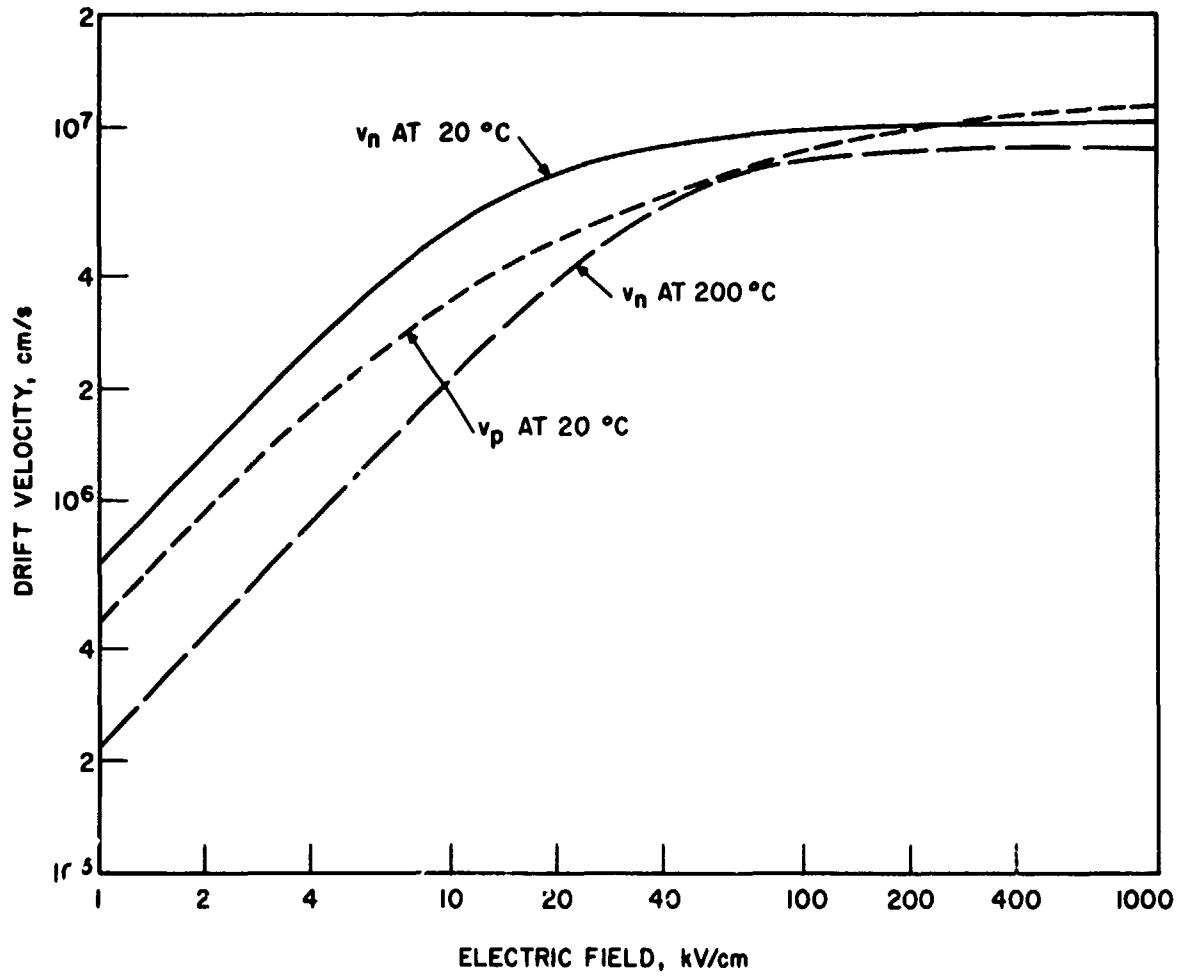


FIG. 7.1 DEPENDENCE OF DRIFT VELOCITY UPON ELECTRIC FIELD FOR ELECTRONS AND HOLES IN Si.

independent of field and equal to $12.5 \text{ cm}^2/\text{s}$ so that the Einstein relationship is satisfied at low field.

Figure 7.2 shows profiles of electric field, hole concentration and particle current density at $\omega t = 90$ degrees, when the total voltage is a maximum, for an operating point of $J_{dc} = 500 \text{ A/cm}^2$ and $V_{RF} = 1 \text{ V}$ at 12 GHz. For the remainder of this section the term profile denotes a function of space at a specific time, e.g., a doping profile, whereas the term waveform denotes a function of time only, e.g., a voltage waveform. From Fig. 7.2 it is apparent that the depletion width is approximately $5.4 \mu\text{m}$ long. The hole concentration is equal to the background doping in the remaining $3.6 \mu\text{m}$ of the active region. This situation is obtained from the direct solution of the hole transport equation, not from the imposition of any additional constraint.

Also in Fig. 7.2 it is seen that the electric field decreases linearly in the depletion region at a rate determined essentially by the background doping. In the adjacent bulk region the field, although it appears to be zero compared to that in the depletion region, is actually uniform at 1.3 kV/cm . This is the value required to maintain constant total current in the finite conductivity bulk region.

Also shown in Fig. 7.2 is the total particle current density which is defined as the sum of the electron and hole current densities. In the drift region the total particle current density is essentially the same as the hole current density since the electron current density is equal to J_{nsat} . The particle current consists of drift and diffusion components which are determined by the local values of hole and electron concentration and the

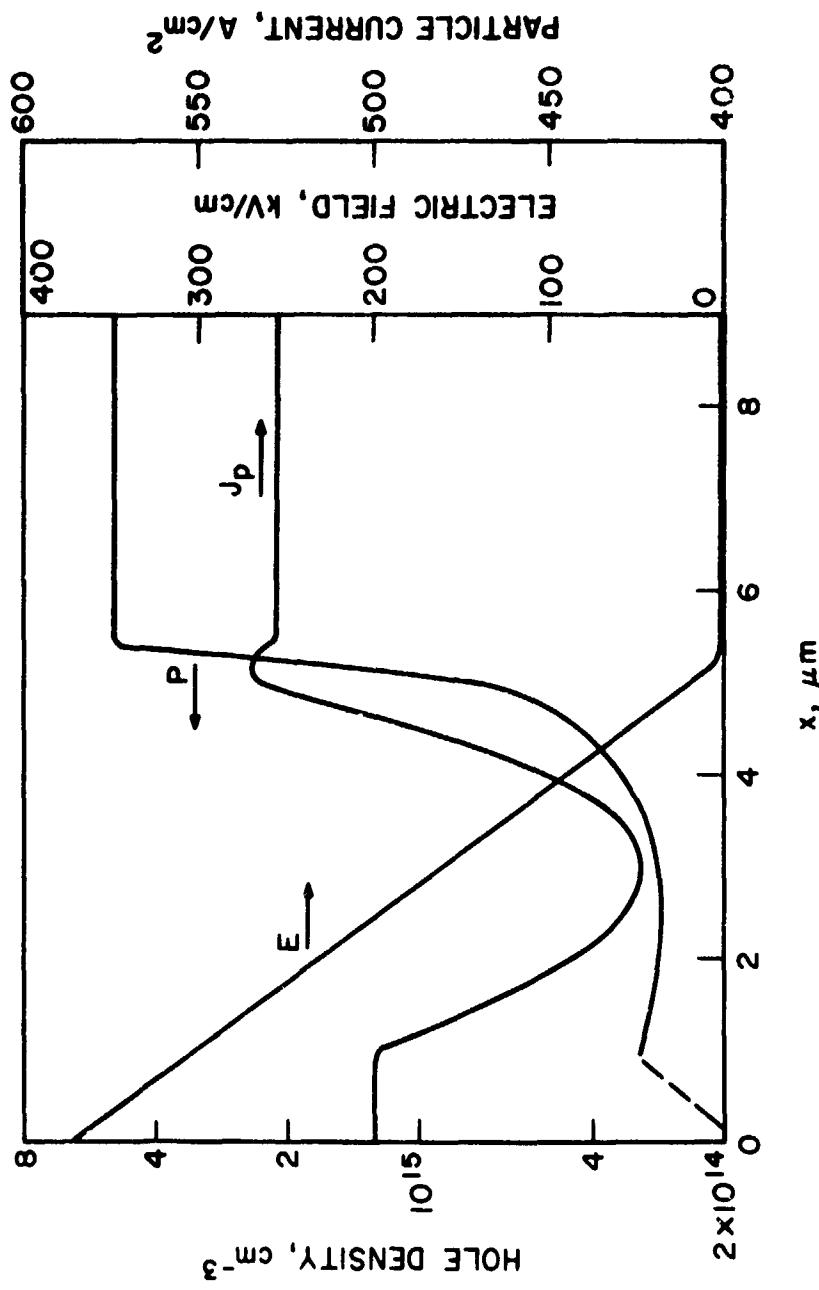


FIG. 7.2 FIELD, PARTICLE CURRENT AND HOLE DENSITY PROFILES AT $\psi_{\text{rf}} = 90$ DEGREES
 FOR A 9- μm Si DIODE. (OPERATING POINT: $V_{\text{rf}} = 1$ V, FREQUENCY = 12
 GHz AND $J_{\text{dc}} = 500$ A/ cm^2)

transport coefficients $v(E)$ and $D(E)$. For later reference the induced current J_{ind} is defined as the space average of the particle current,

$$J_{ind}(t) = \frac{1}{l} \int_0^l J_p(x, t) dx , \quad (7.3)$$

and is a function of time only. Because the scales of Fig. 7.2 were chosen to show the full range of E and p values and because the operating point under consideration is essentially small signal, the profiles for other time instants appear very similar to Fig. 7.2.

Figure 7.3 shows the time-domain waveforms obtained for this operating point. The RF voltage is taken to be a 1-V sinusoid. The resulting current waveforms are seen to be approximately sinusoidal also. The injected current is defined as the particle current at the interface of the avalanche and drift regions, i.e., $x = 1 \mu\text{m}$ in this case. The injected current is seen to lag the voltage by 81 degrees. The induced current lags the injected current by 177 degrees. The device admittance determined from the total current (which is the sum of the induced current and the capacitive current for the entire active region) is $Y = -15.5 + j127 \text{ mho/cm}^2$.

In Fig. 7.3 the induced current was seen to lag the injected current by an angle much larger than one half of the effective transit angle of the depletion region. This is because the particle current in the bulk region contributes to the induced current. For the sake of comparison another n^+pp^+ diode was modeled; it is identical in all respects with the previous one except that the p-layer thickness was taken to be $5 \mu\text{m}$ so that the diode is punched through at breakdown (see Fig. 7.2). The computed current waveforms for this case are plotted in Fig. 7.4. The injected current is

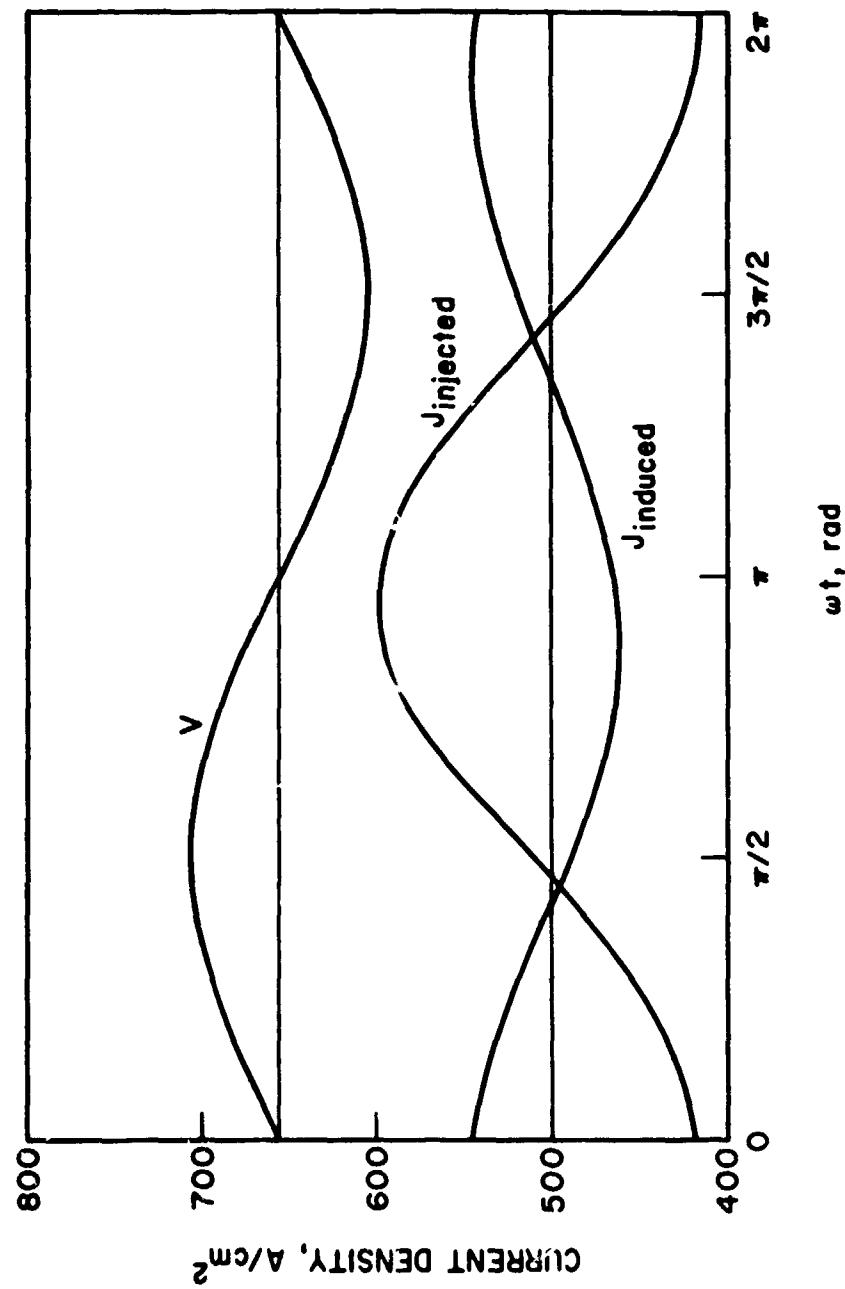


FIG. 7.3 WAVEFORMS OF INJECTED AND INDUCED CURRENT DENSITY FOR A 9- μ m Si DIODE.
 (OPERATING POINT: $V_{RF} = 1$ V, FREQUENCY = 12 GHz AND $J_{dc} = 500$ A/cm 2)

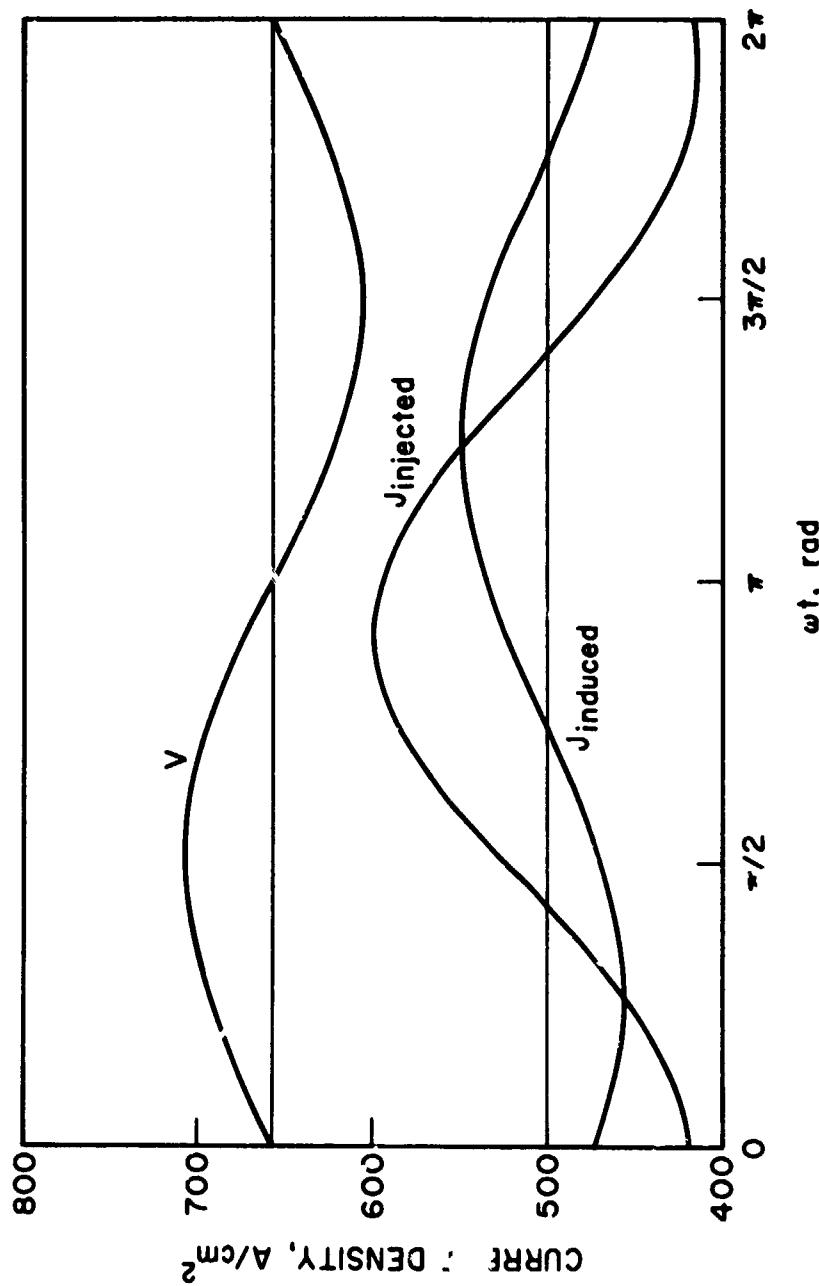


FIG. 7.4. WAVEFORMS OF INJECTED AND INDUCED CURRENT DENSITY FOR A 5- μm Si DIODE. (OPERATING POINT: $V_{\text{RF}} = 1$ V, FREQUENCY = 12 GHz AND $J_{\text{dc}} = 500$ A/cm²)

seen to lag the voltage by 75 degrees. The induced current lags the injected current by 60 degrees which is one half of the effective transit angle of the depletion region. The computed device admittance is $Y = -33.5 + j126 \text{ mho/cm}^2$. Observe that the negative conductance is larger by a factor of two than for the unswept epitaxial case.

The difference between the device admittances calculated for these two cases is due to the presence of 4 μm of bulk p-region in the former case which acts essentially as a series resistance. If the low-field mobility and a hole concentration equal to the background doping are used, a resistance of $1.04 \text{ m}\Omega \text{ cm}^2$ is found. When this value is placed in series with the device admittance computed for the 5- μm diode, a total admittance of $Y = -17 + j132$ is obtained. This is in close agreement with the value actually computed for the 9- μm diode.

The point of this comparison is to show that the computer program can handle nonpunch-through diodes by extending the active region into the bulk. In this case the answer obtained shows that the bulk region has the effect of a series resistance, in agreement with physical intuition. In cases of large voltage modulation this approach is felt to be superior to simply adding on an effective resistance.

7.3 Silicon Abrupt-Junction Diodes with 5×10^{15} Background Doping.

For this case the structures under consideration are p^+nn^+ and n^+pp^+ Si diodes with a uniform background doping of $5 \times 10^{15} \text{ cm}^{-3}$ in the lightly doped region. Further, the width of the lightly doped region is 5 μm in both cases so that the two diode structures are complementary. Both diodes are punched through prior to breakdown.

To facilitate the comparison with other diode analyses, to be described later, diffusive transport was neglected and the velocities of electrons and holes were taken to be constant, independent of the field and equal to 10^7 cm/s.

7.3.1 Small-Signal Analysis. An analysis has recently been developed (see Section 6) which calculates the "exact" small-signal admittance for a given diode structure. It is restricted to small signal since it performs linear perturbations upon the static current and field profiles; these are obtained from a static analysis described previously.² However, it requires no a priori assumption about the localization of the impact ionization and it handles unequal ionization rates and drift velocities for electrons and holes (the drift velocities are assumed constant).

Figure 7.5 shows the small-signal admittance curves obtained from the exact analysis for the complementary Si diodes biased at 500, 1000 and 2000 A/cm². It is seen that at each bias current level the peak negative conductance is about 50 percent larger for the p-type than for the n-type diode. This is due to the inequality of the ionization rates, which results in a narrower avalanche region for the p-type structure as has been discussed previously.³

In order to model the complementary Si diodes with the large-signal analysis of this section, it is necessary to select the effective avalanche

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2. Schroeder, W. E. and Haddad, G. I., "Avalanche Region Width in Various Structures of IMPATT Diodes," Proc. IEEE (Correspondence), vol. 59, No. 8, pp. 1245-1248, August 1971.
 3. Gilden, M. and Hines, M. E., "Electronic Tuning Effects in Read Microwave Avalanche Diodes," IEEE Trans. on Electron Devices, vol. ED-13, No. 1, pp. 169-175, January 1966.

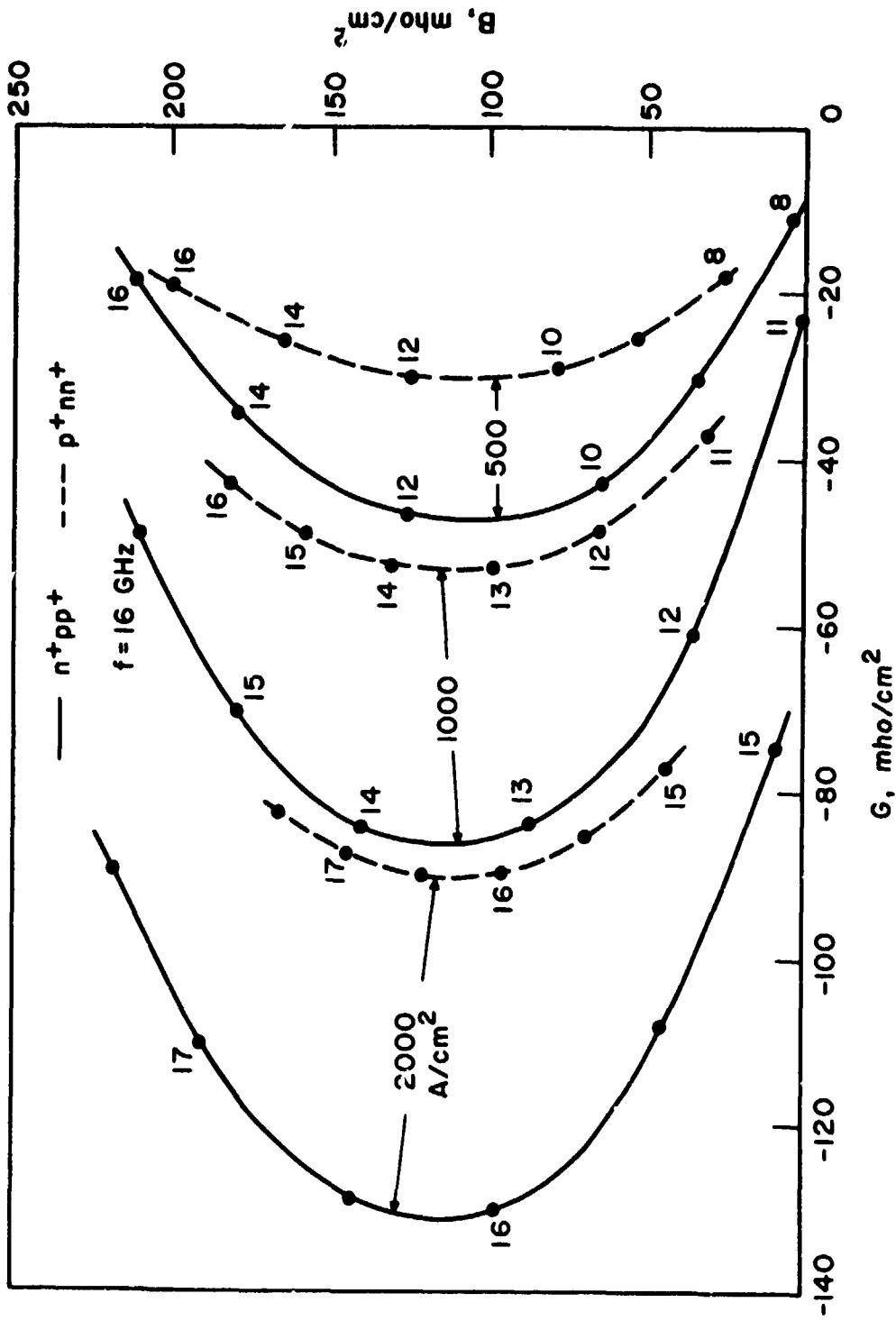


FIG. 7.5 SMALL-SIGNAL ADMITTANCE DETERMINED FROM THE EXACT ANALYSIS FOR COMPLEMENTARY Si DIODES.
(BACKGROUND DOPING = $5 \times 10^{15} \text{ cm}^{-3}$ AND WIDTH = 5 μm)

region width appropriately. Previously, using a somewhat arbitrary definition of avalanche width, i.e., the region where 95 percent of the particle current is generated, effective avalanche widths of 17 and 40 percent were established for p- and n-type diodes of this doping level, respectively. In view of the arbitrariness of the 95 percent criterion, it was decided to make a direct comparison of the small-signal admittance calculated from the exact analysis with that obtained from the localized avalanche model using different effective avalanche widths. Since for the case of constant velocity and no diffusion the localized avalanche model reduces to the familiar Read model, an analytic expression is obtained for the small-signal admittance:³

$$Y_{GH} = j \frac{\omega}{l} \left[\frac{1 - \left(\frac{\omega^2}{\omega_a^2} \right)}{\left(\frac{l_d}{l} - \frac{\omega^2}{\omega_a^2} \right) + j\beta \left(\frac{l_d}{l} \right)} \right], \quad (7.4)$$

where l = the total length of the active region,

l_d = the length of the drift region,

ω_a = the avalanche resonant frequency,

$\beta \triangleq [1 - \exp(-j\omega\tau_d)]/\omega\tau_d$ and

$\tau_d \triangleq l_d/v_{sat}$.

Thus the effect of different avalanche widths is easily determined from evaluation of Eq. 7.4. The avalanche resonant frequency is determined by the avalanche width as well as the ionization rates.

Figure 7.6 shows this comparison for the p^+nn^+ diode biased at 500 A/cm^2 . Observe that the exact admittance curve does not pass through

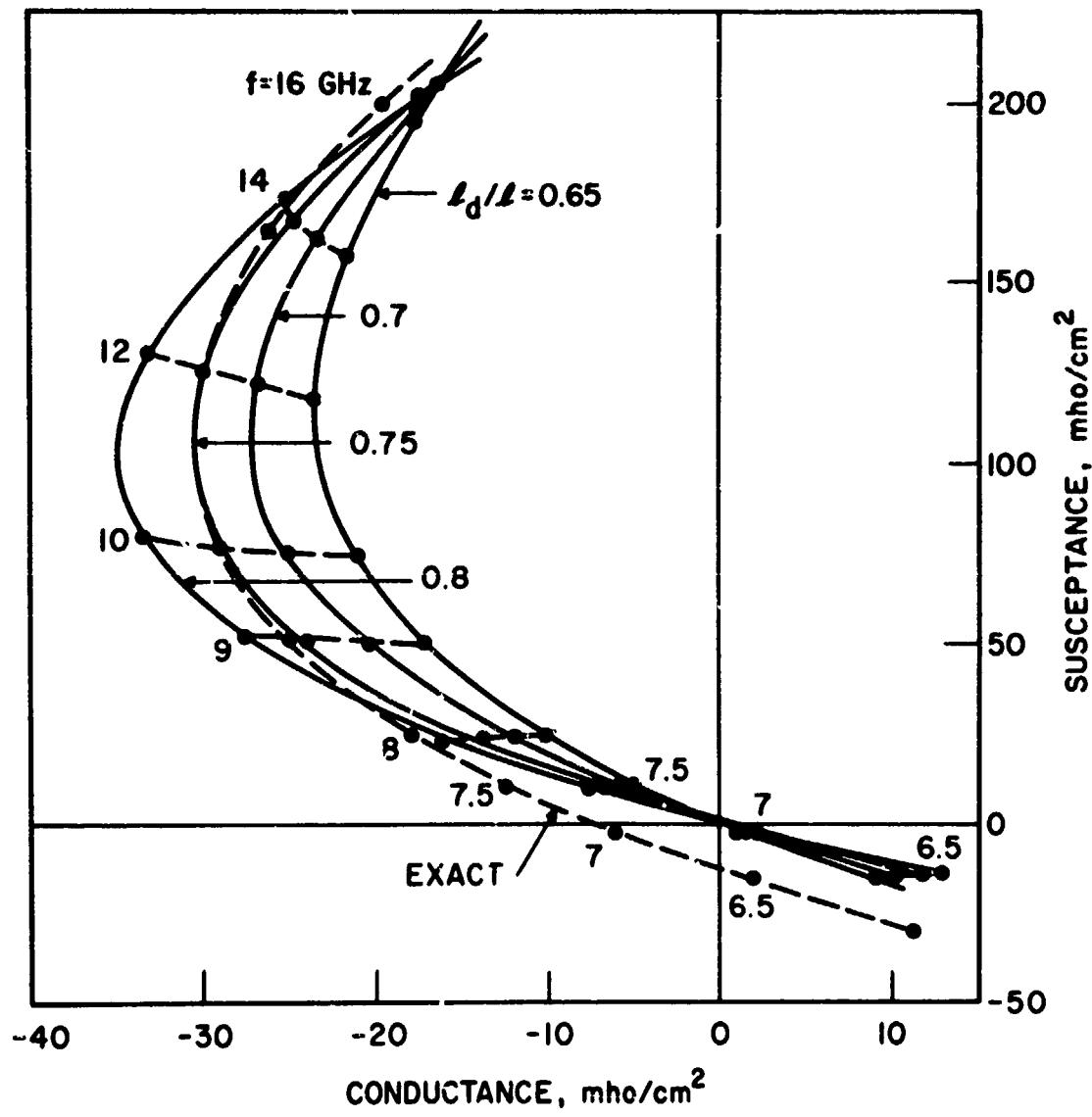


FIG. 7.6 COMPARISON OF EXACT SMALL-SIGNAL ADMITTANCE WITH THE APPROXIMATE READ DIODE EXPRESSION FOR A 5- μ m p^+nn^+ Si DIODE BIASED AT 500 A/cm². (AVALANCHE RESONANT FREQUENCY = 7.1 GHz AND $l_d/l \triangleq$ FRACTIONAL DRIFT LENGTH)

the origin of the admittance plane. The conductance and susceptance change sign at approximately 6.6 GHz and 7.1 GHz, respectively. On the other hand, the Read model admittance curves all pass through the origin at $f = f_a$, as may be seen from inspection of Eq. 7:4. Thus, no matter what choice of l_d/l and f_a is made, the curves cannot be in complete agreement near the avalanche frequency. However, the frequencies which are generally of the most interest are those where peak negative conductance occurs; here the agreement can be made excellent as shown in the figure.

In Fig. 7.6 the avalanche frequency is taken to be 7.1 GHz for all of the Read model curves. It is seen that the effect of widening the avalanche region is to reduce the peak negative conductance substantially and to increase somewhat the frequency for peak-G concomitant with the reduced drift region length. Although it is not shown in the figure, the effect of increasing avalanche frequency while maintaining fractional avalanche width constant is to increase the peak negative conductance. Of course, the frequency at which the admittance zero occurs is equal to the avalanche frequency.

It is seen in Fig. 7.6 that a choice of $l_d/l = 0.75$ gives good agreement between the Read admittance curve and the exact admittance, particularly near the peak negative conductance frequencies. This corresponds to a fractional avalanche width of 25 percent or $1.25 \mu\text{m}$. A similar comparison was made for this diode operated at 2000 A/cm^2 and again good agreement was obtained with the exact curve using an avalanche frequency increased by a factor of two (square root of the current ratio) and an avalanche width of 25 percent. Thus $x_a = 1.25 \mu\text{m}$ is used in the remainder of this section for the $\text{p}^+ \text{nn}^+$, $5 \times 10^{15} \text{ cm}^{-3}$ Si diode. Similar comparisons were carried out for

the complementary n^+pp^+ diode and yielded a narrower effective avalanche region equal to 15 percent of the total depletion width or $0.75 \mu\text{m}$; this value is used subsequently for the large-signal calculations.

7.3.2 Large-Signal Analysis. Recently, a large-signal diode analysis has been developed in connection with a study of the high-efficiency mode, which also may be used for studying the IMPATT mode.⁴ It permits distributed ionization and requires saturated velocities as does the exact small-signal analysis. Under small drive conditions it computes admittance values in good agreement with those from the exact small-signal analysis; since the programs are independent this agreement serves as a validity check. It is of interest to compare the results of this program with those from the localized avalanche model of this section. For ease of identification the models will be referred to as distributed and Read, respectively.

For the remainder of Section 7.3.2 the operating point of the complementary Si diodes will be restricted to a bias current of 1200 A/cm^2 and an operating frequency of 14 GHz , which is near optimum at large signal. Figure 7.7 shows the device admittance as a function of the RF voltage level computed for the Read model for the complementary Si diodes. It is seen that at small signal the negative conductance for the n^+pp^+ diode is about 50 percent larger than for the complement, that the negative conductance decreases monotonically with voltage for both and that at 50 V the p-type has a negative conductance only 20 percent larger than the n-type. The susceptance for both diodes increases with voltage, approaching the depletion layer capacitance value at large drive levels.

4. Haddad, G. I. et al., "Microwave Solid-State Device and Circuit Studies," Quarterly Progress Report No. 3, Contract No. F30602-71-C-0099, Electron Physics Laboratory, The University of Michigan, Ann Arbor, June 1971.

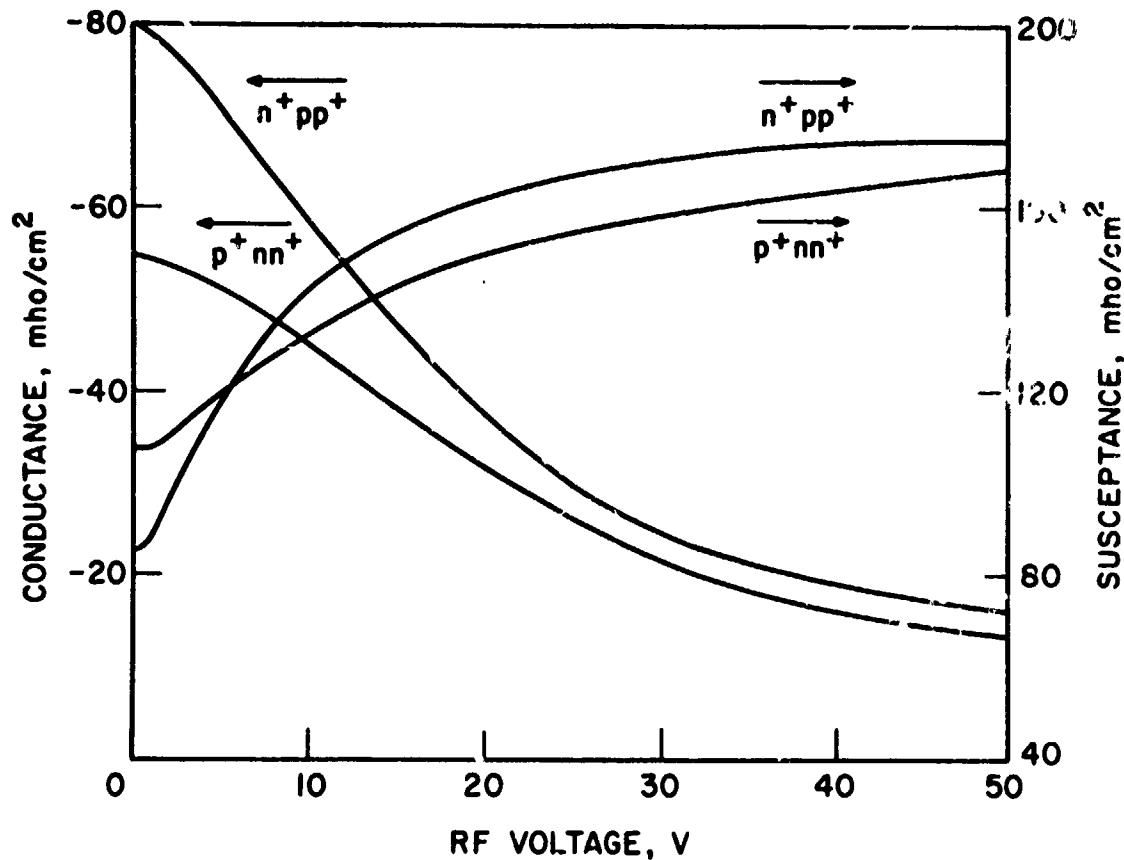


FIG. 7.7 DEVICE ADMITTANCE AS A FUNCTION OF RF LEVEL FOR THE COMPLEMENTARY Si DIODES. (BACKGROUND DOPING = $5 \times 10^{15} \text{ cm}^{-3}$ AND WIDTH = 5 μm . OPERATING POINT: FREQUENCY = 14 GHz AND $J_{dc} = 1200 \text{ A/cm}^2$)

Figure 7.8 compares the induced current waveforms computed from the distributed and Read models for the n^+pp^+ diode at $V_{RF} = 50$ V. They are seen to be in very good agreement and consequently the diode admittance values are also. The Read model admittance is $Y = -15.9 + j174$ and the distributed model value is $Y = -16.3 + j177.6 \text{ mho/cm}^2$. In Fig. 7.8 it is seen that the agreement is very good for the portion of time when the induced current rises from a low value to the peak value; this, of course, is the time when avalanche generation of carriers takes place. The hump in induced current slightly before 180 degrees is due to the contribution of electron current. After about 200 degrees the induced current is constant because all the electrons have been collected and the hole pulse is drifting at constant velocity. Slightly before 360 degrees the hole pulse begins to be collected at the far end of the drift region.

Figure 7.9 shows the particle current profile at several times in the RF cycle calculated from the Read model for the same operating point as Fig. 7.8. The four time instants shown correspond to the generation and launch of the hole current pulse. Figure 7.10 compares the particle current profiles at $\omega t = 180$ degrees obtained from the Read and distributed models. In the distributed model the particle current is found to be nonuniform in the avalanche region. Also, the hole pulse in the distributed model lags that of the Read model by $0.25 \mu\text{m}$, which corresponds to the hole pulse being launched from the middle of the effective avalanche region.

Figure 7.11 compares the induced current waveforms calculated from the two models for the p^+nn^+ diode at $V_{RF} = 50$ V, i.e., the case complementary to Fig. 7.8. The waveforms are seen to be very similar in shape but the induced current from the distributed model lags the other by about 15 degrees.

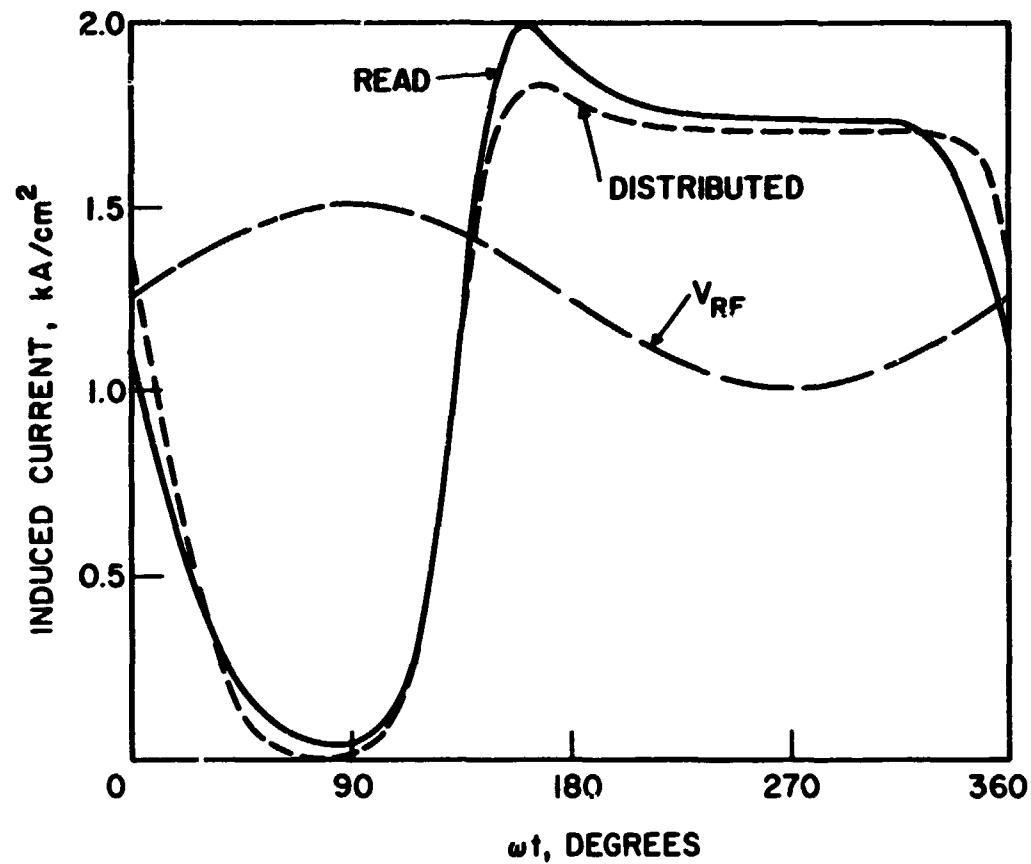


FIG. 7.8 COMPARISON OF INDUCED CURRENT WAVEFORMS DETERMINED BY THE LARGE-SIGNAL MODELS FOR A 5- μ m n^+pp^+ , $5 \times 10^{15} \text{ cm}^{-3}$ DIODE. (OPERATING POINT: $V_{RF} = 50 \text{ V}$, FREQUENCY = 14 GHz AND $J_{dc} = 1200 \text{ A/cm}^2$)

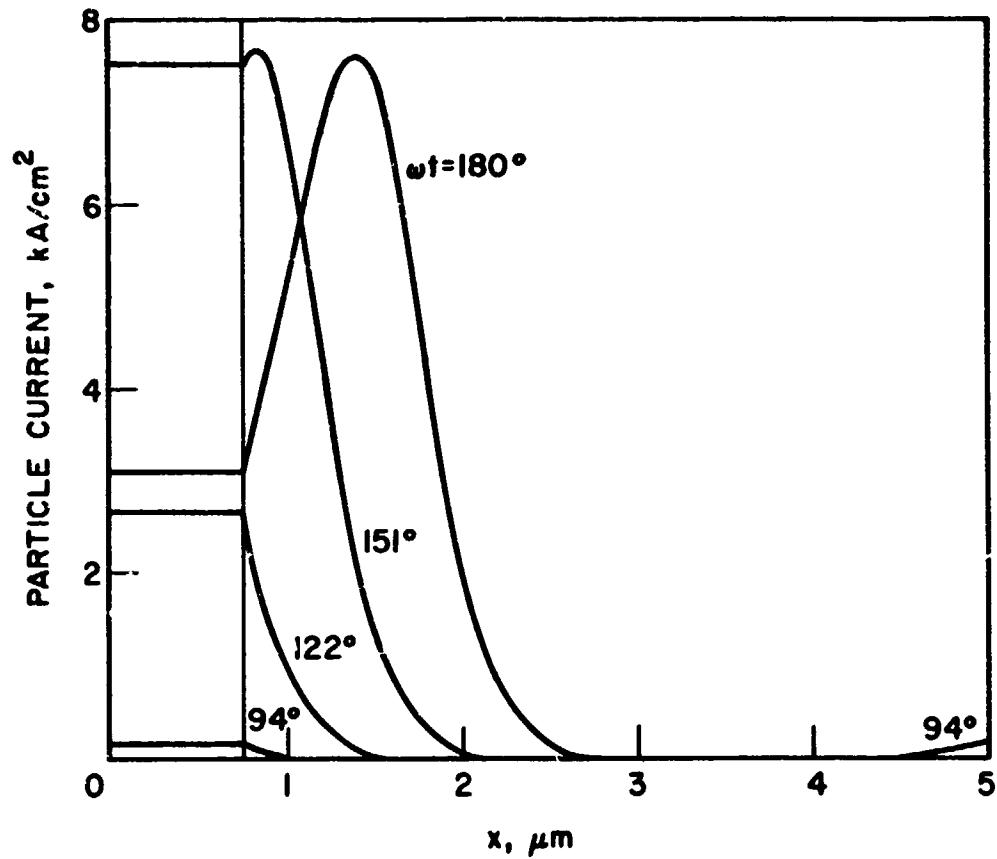


FIG. 7.9 PARTICLE CURRENT PROFILES AT SEVERAL TIMES IN THE RF CYCLE FOR A 5- μm n^+ pp^+ , $5 \times 10^{15} \text{ cm}^{-3}$ DIODE. (OPERATING POINT: $V_{RF} = 50 \text{ V}$, FREQUENCY = 14 GHz AND $J_{dc} = 1200 \text{ A/cm}^2$)

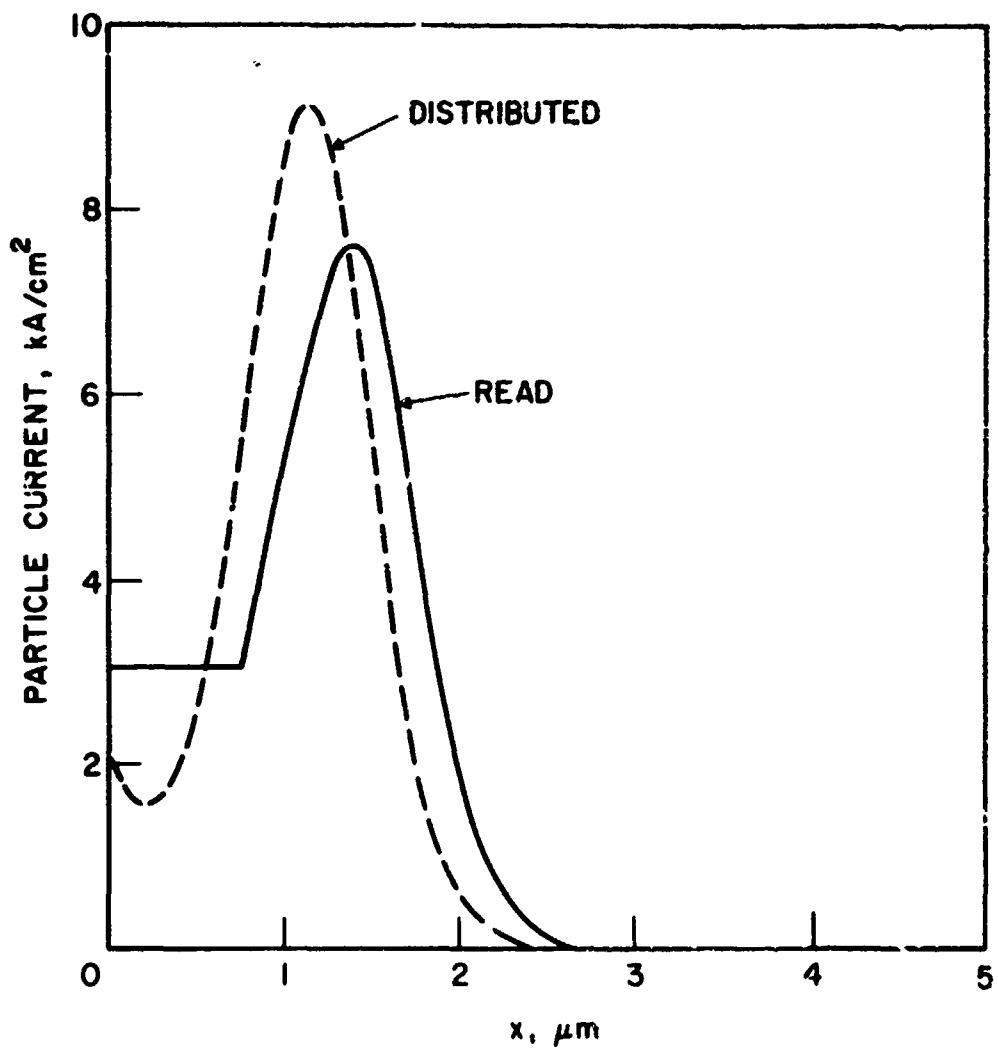


FIG. 7.10 COMPARISON OF PARTICLE CURRENT PROFILES AT $\phi_i = 180$ DEGREES
DETERMINED BY THE LARGE-SIGNAL MODELS FOR A $5\text{-}\mu\text{m}$ n^+pp^+ , 5×10^{15}
 cm^{-3} DIODE. (OPERATING POINT: $V_{RF} = 50$ V, FREQUENCY = 1^h GHz
AND $J_{dc} = 1200 \text{ A/cm}^2$)

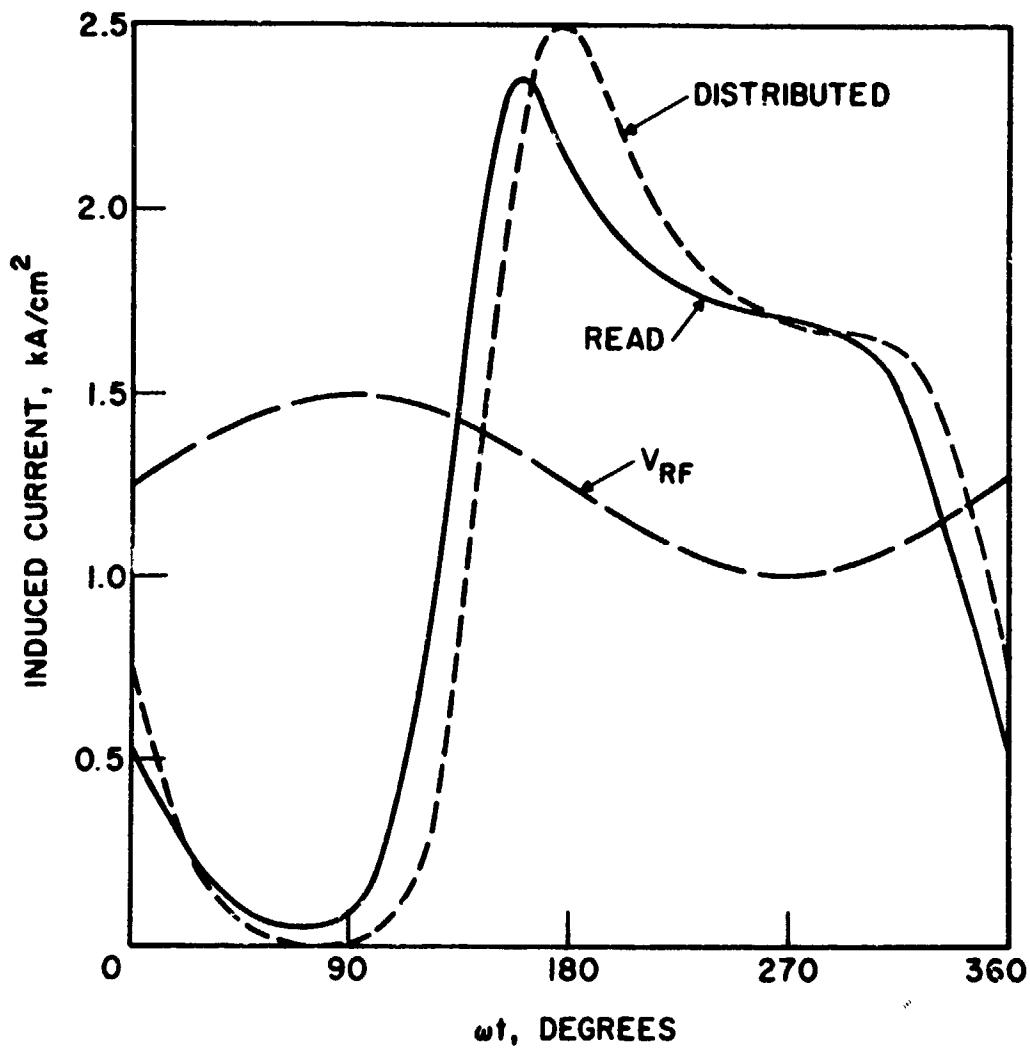


FIG. 7.11 COMPARISON OF INDUCED CURRENT WAVEFORMS DETERMINED BY THE LARGE-SIGNAL MODELS FOR A 5- μm p^+nn^+ , $5 \times 10^{15} \text{ cm}^{-3}$ DIODE. (OPERATING POINT: $V_{RF} = 50 \text{ V}$, FREQUENCY = 14 GHz AND $J_{ac} = 1200 \text{ A/cm}^2$)

As a result the admittances do not agree as closely as in the complementary case. The admittances computed are $Y = -13.4 + j168 \text{ mho/cm}^2$ and $Y = -17.9 + j171 \text{ mho/cm}^2$ for the Read and distributed models, respectively. Again, the hump in induced current near 180 degrees is due to "minority" carrier current, in this case holes. The hump is more pronounced than in Fig. 7.8 because the avalanche region is wider.

As we have already seen in the small-signal case, negative conductance decreases with increasing avalanche width. In the two large-signal cases just described smaller negative conductance was calculated from the Read model for 25 percent than for 15 percent effective avalanche widths. This appears to be a general property of the Read model as is shown in Fig. 7.12; here large-signal admittances are shown which were calculated for a diode of 5 μm total length and various avalanche widths. The operating point for all cases is $V_{\text{RF}} = 50 \text{ V}$, frequency = 14 GHz and $J_{d1} = 1200 \text{ A/cm}^2$. The avalanche widths other than 15 and 25 percent do not necessarily correspond to any particular diode structure but rather are used to show the effect of the avalanche width parameter in the model.

Table 7.1 summarizes the results obtained from the two models for the complementary Si diodes at the 14 GHz, 50 V RF, 1200 A/cm² operating point. For the p-type diode the two models give results which are in excellent agreement; the calculated efficiency is slightly less than 20 percent. For the n-type diodes the two models differ somewhat as described previously. However, what may be more important than the difference is that either model predicts that the efficiency is not greatly different from that of the complementary diode, e.g., two percent less in the Read model vs. two percent more in the distributed model. Two

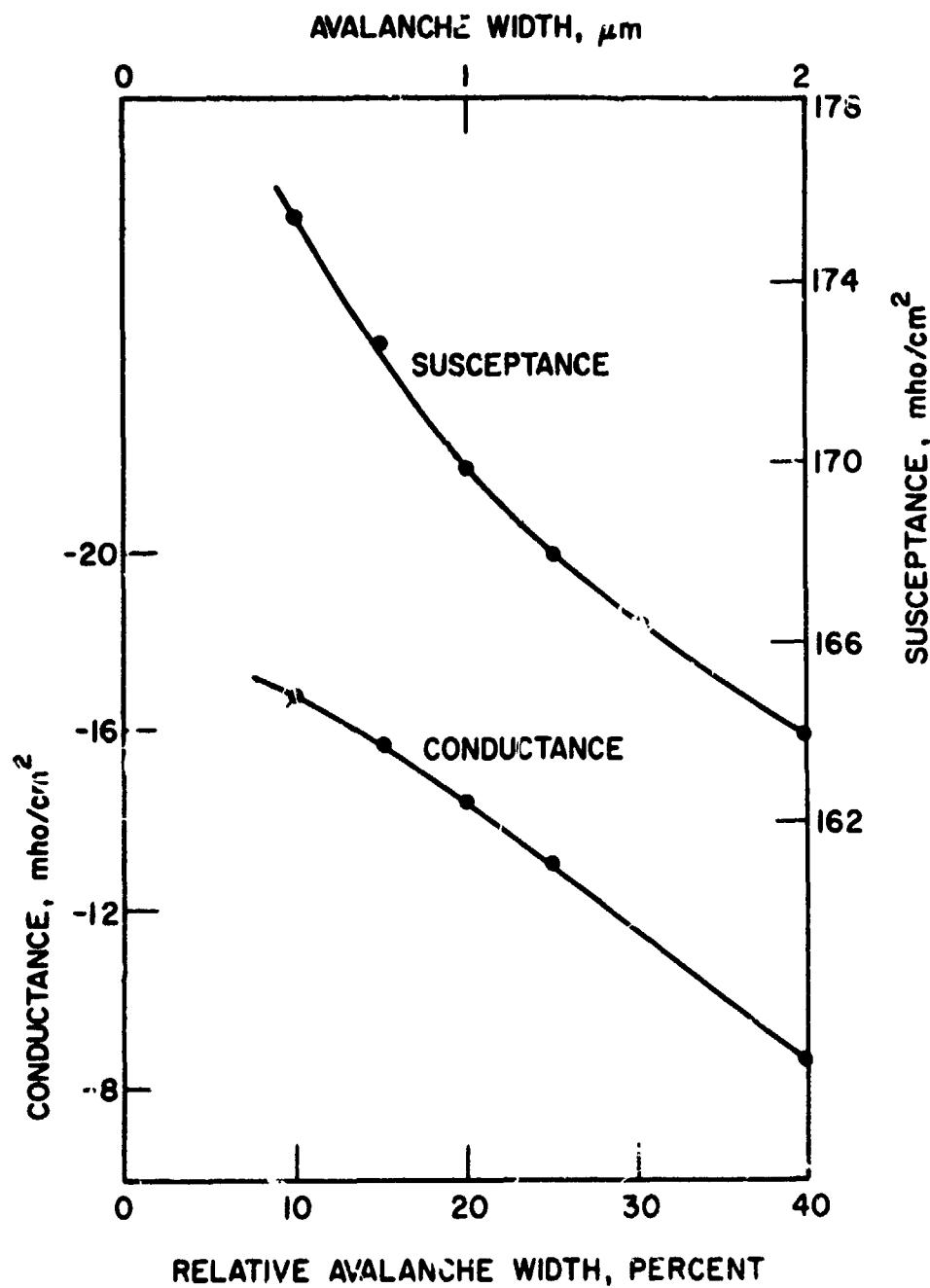


FIG. 7.12 DEPENDENCE OF LARGE-SIGNAL ADMITTANCE UPON EFFECTIVE AVALANCHE WIDTH FOR A DIODE WITH TOTAL WIDTH = 5 μ m. (OPERATING POINT: $V_{RF} = 50$ V, FREQUENCY = 14 GHz AND $J_{dc} = 1200$ A/cm²)

qualifications should be noted with respect to the efficiency values quoted here. First, the operating point is not necessarily that which yields peak efficiency for either structure. Second, the efficiencies quoted are optimistic since in both models the field in the drift region was computed to be very small near $\omega t = 270$ degrees which would lead to a smaller induced current if the velocities were permitted to become unsaturated.

Table 7.1
Large-Signal Data for Complementary Diodes

Type	Model	G(mho/cm ²)	B(mho/cm ²)	V _{dc} (v)	P _{RF} (kW/cm ²)	η (%)
n ⁺ pp ⁺	Read	-15.9	174	84.5	19.9	19.7
n ⁺ pp ⁺	distributed	-16.3	177.6	85.4	20.4	19.9
p ⁺ nn ⁺	Read	-13.4	167.5	76.5	16.7	18.2
p ⁺ nn ⁺	distributed	-17.9	170.8	85.3	22.4	22.3

7.4 Millimeter-Wave Silicon Diodes. The diode structure under consideration in this section is a one-sided, p⁺nn⁺ Si junction with n-region doping of 7×10^{16} cm⁻³ and width of 0.50 μ m. The dc current is taken equal to 10^4 A/cm² in all cases. Material parameters appropriate to Si at 200°C are used throughout.

The small-signal admittance of this structure was evaluated using the exact analysis mentioned in the previous section. For the purpose of this analysis the velocities of electrons and holes were taken to be constant and equal to 8.8×10^6 cm/s. Since the diode is punched through at breakdown with a minimum field of 9.8×10^4 V/cm, this is a reasonable approximation for the static and small-signal case. The ionization rates were taken to be of the form $A[\exp(-b/E)]$, where for electrons

$A = 1.08 \times 10^6 \text{ cm}^{-1}$ and $b = 1.34 \times 10^6 \text{ V/cm}$ and for holes $A = 2.56 \times 10^6 \text{ cm}^{-1}$ and $b = 2.44 \times 10^6 \text{ V/cm}$. These values⁵ are believed to be appropriate to Si at high fields ($\sim 6 \times 10^5 \text{ V/cm}$) and 200°C. Figure 7.13 shows the exact small-signal admittance which was computed using these parameters. The frequencies for zero conductance and susceptance are 35 and 42 GHz, respectively. The breakdown voltage was found to be 16.9 V with low current and 17.2 V at the operating current of 10^4 A/cm^2 .

The analytic small-signal admittance expression of Eq. 7.4 was evaluated for several choices of avalanche width and avalanche resonant frequency. A relative avalanche width of 30 percent (or $0.150 \mu\text{m}$) and an avalanche frequency of 38 GHz were found to give a good fit; the resulting admittance is also plotted in Fig. 7.13. Observe that the effective avalanche width is wider than for the n-type X-band Si diode; this is because the ionization rates are flatter at high field which leads to a spread out generation region.³

Using the large-signal, localized avalanche computer program, values for device admittance were computed as a function of frequency and voltage level and are shown in Fig. 7.14. For this program the drift velocity of electrons was taken to have the field dependence shown in Fig. 7.1; the saturated value is $8.8 \times 10^6 \text{ cm/s}$ and the low-field mobility is $220 \text{ cm}^2/\text{V-s}$. The diffusion coefficient was taken to be field independent and equal to $9 \text{ cm}^2/\text{s}$ in agreement with the Einstein relationship at low field. An effective ionization rate was determined which gives the desired breakdown voltage and avalanche resonant frequency; it is close to that of electrons.

5. Bowman, L., private communication.

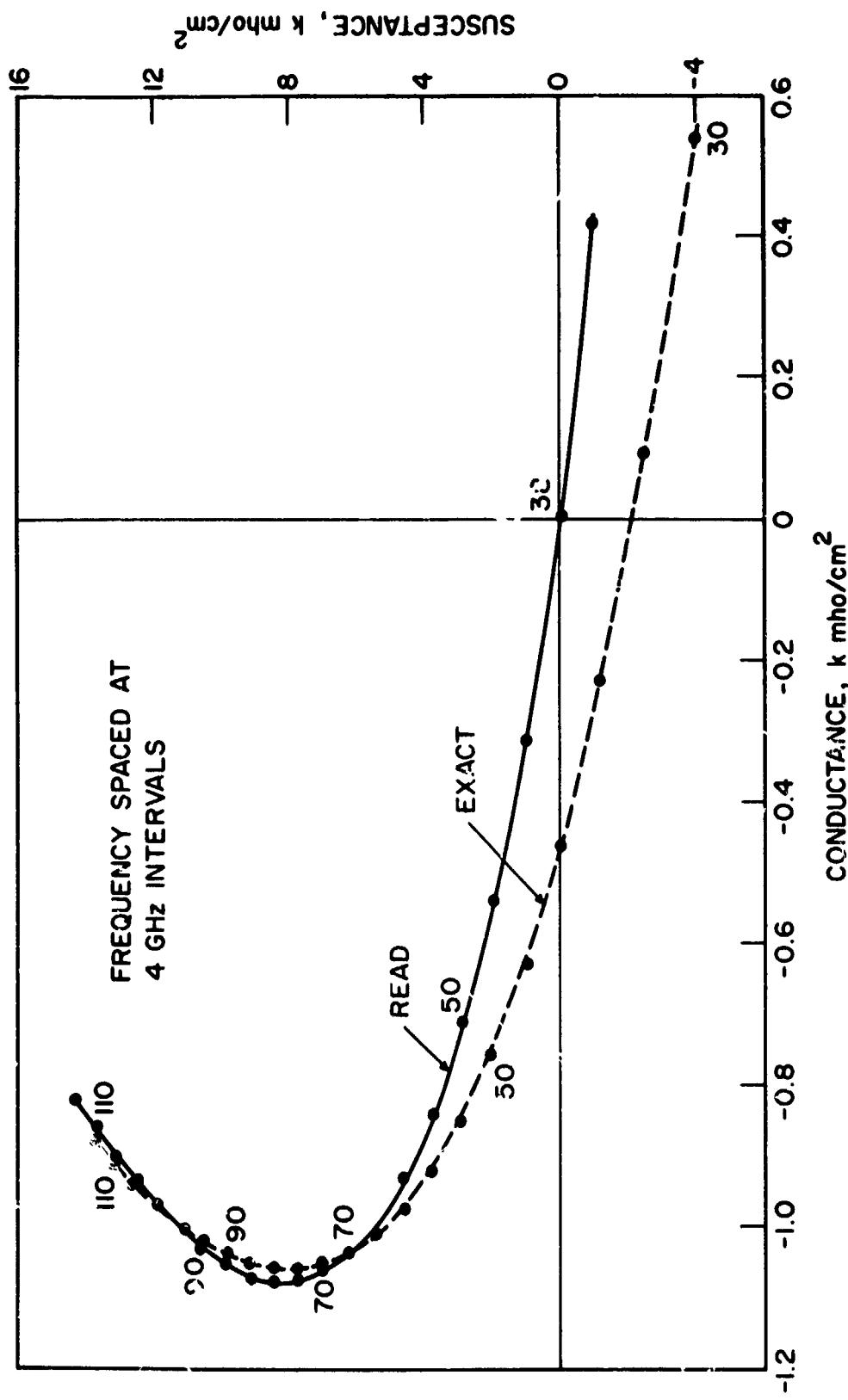


FIG. 7.13 COMPARISON OF EXACT SMALL-SIGNAL ADMITTANCE WITH THE APPROXIMATE READ-DIODE EXPRESSION
 FOR A $0.5\text{-}\mu\text{m } p^+nn^+p^+$ Si DIODE BIASED AT 10^4 A/cm^2 . (AVALANCHE RESONANT FREQUENCY = 38 GHz
 AND RELATIVE AVALANCHE WIDTH = 30 PERCENT)

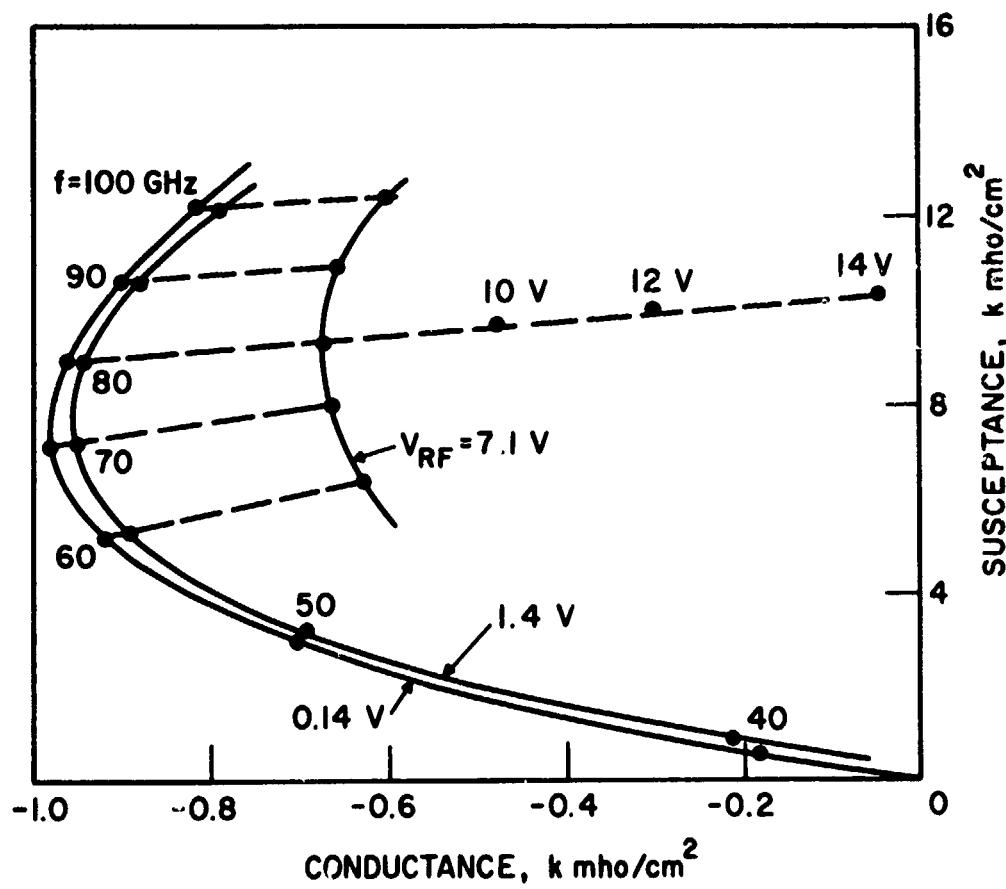


FIG. 7.14 DEVICE ADMITTANCE AS A FUNCTION OF FREQUENCY AND RF VOLTAGE FOR A $0.5\text{-}\mu\text{m } \text{p}^+\text{nn}^+$ Si DIODE BIASED AT 10^4 A/cm^2 .

In Fig. 7.1^b the $V_{RF} = 0.14$ curve corresponds to small signal since the computed ac current was found to be sinusoidal and very small compared to the dc. It is in good agreement with the small-signal admittance shown in Fig. 7.13 which was computed from Eq. 7.4, except that the peak negative conductance here is slightly smaller. This difference is attributed to the effects of unsaturated velocity and diffusion which were not incorporated in Eq. 7.4. The curve for $V_{RF} = 1.4$ V is seen to be near the beginning of the nonlinear regime because it differs only slightly from that for $V_{RF} = 0.14$ V. For voltages above 7.1 V data were taken only for $f = 80$ GHz.

Figure 7.15 shows the power and efficiency calculated at $f = 80$ GHz as a function of RF voltage. It is seen that power and efficiency saturate at approximately 10 V and then decrease with increased drive level. The peak efficiency calculated is 14.1 percent. The power and efficiency saturate because the induced current waveform develops a dip at approximately 270 degrees. The size of the dip increases with voltage level as shown in Fig. 7.16. Because the dip occurs at the time when the RF voltage is minimum it seriously degrades the generated RF power.

The cause of the dip is shown in Fig. 7.17 which gives the electric field and electron concentration profiles for several time instants at the 14-V operating point. It is seen that the electric field in the drift region becomes negative which results in the electrons drifting opposite to the normal direction. Also, electrons flow into the drift region from the contact which normally collects electrons, in what is essentially depletion layer width modulation. Both of these processes give negative particle current which is manifested as the dip in induced current.

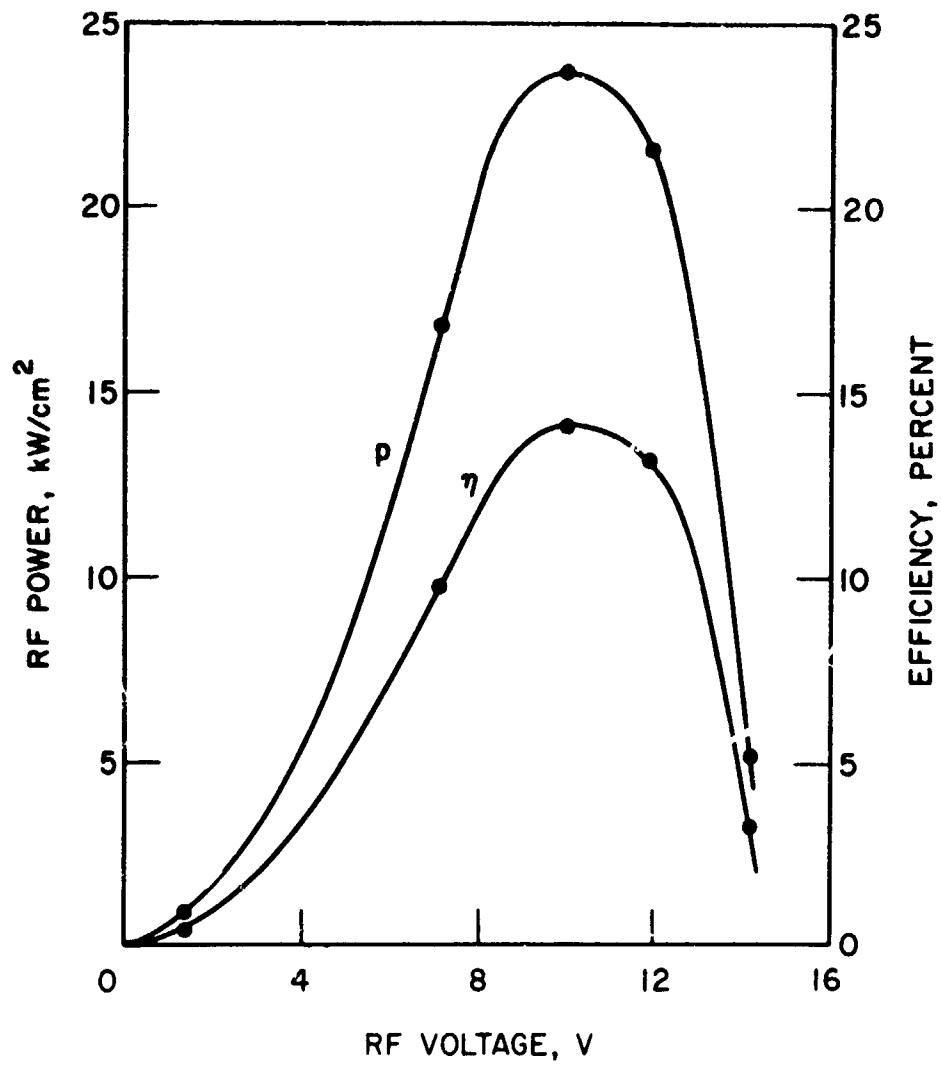


FIG. 7.15 POWER AND EFFICIENCY AS A FUNCTION OF RF LEVEL FOR A 0.5- μ m $p^{+}nn^{+}$ Si DIODE. (OPERATING POINT: FREQUENCY = 80 GHz AND $J_{dc} = 10^4$ A/cm²)

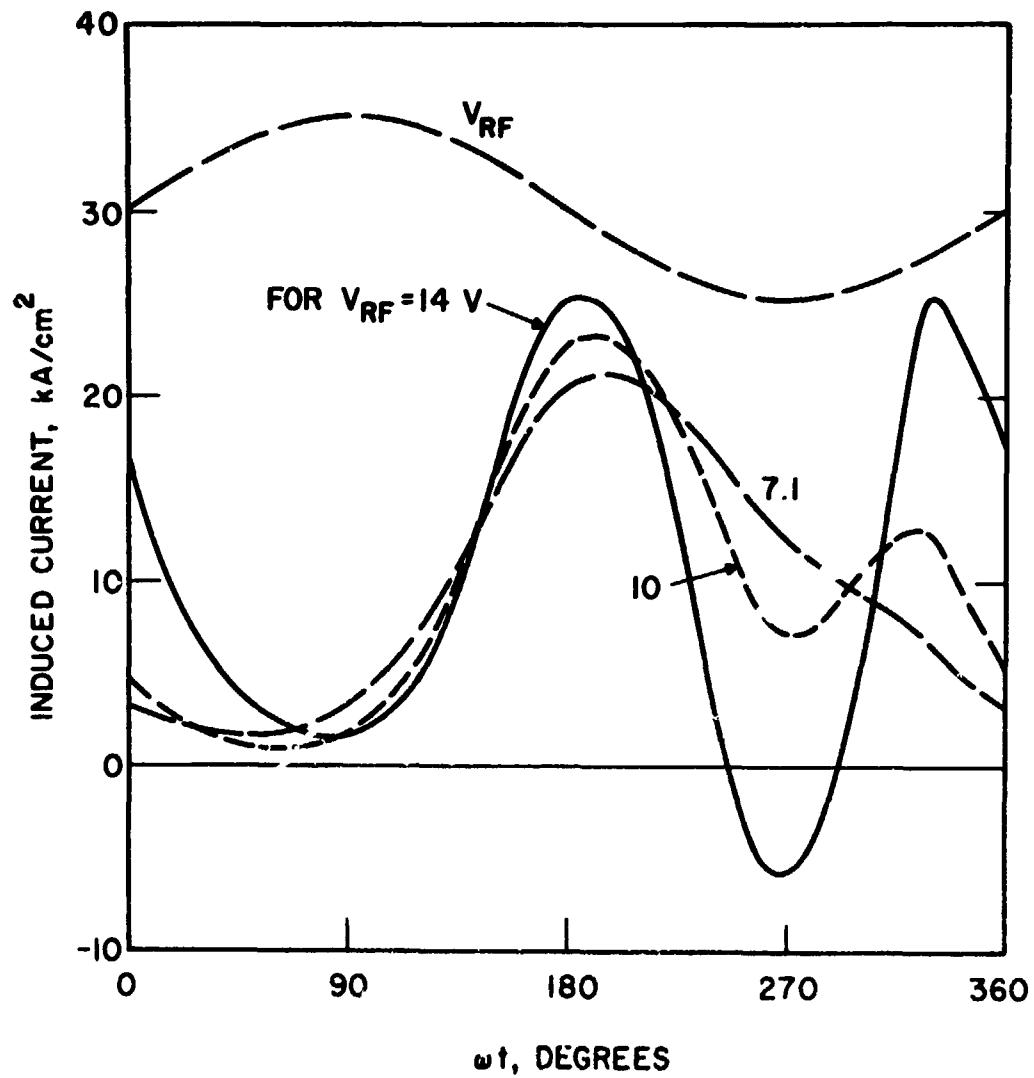


FIG. 7.16 COMPARISON OF INDUCED CURRENT WAVEFORMS AT SEVERAL RF LEVELS FOR A 0.5- μ m p^+nn^+ Si DIODE. (OPERATING POINT: FREQUENCY = 80 GHz AND $J_{dc} = 10^4$ A/cm 2)

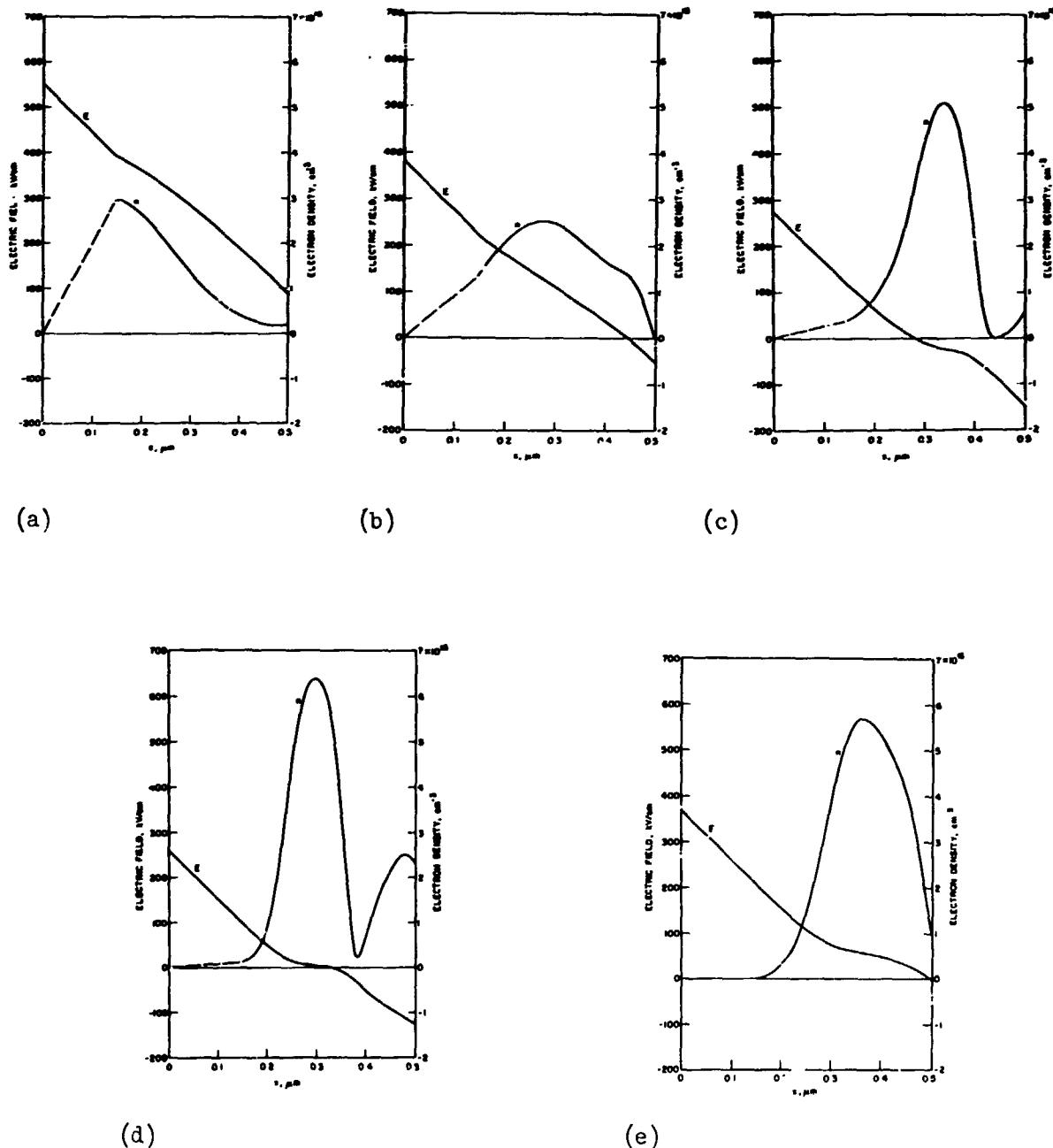


FIG. 7.17 ELECTRIC FIELD AND ELECTRON DENSITY PROFILES AT SEVERAL TIMES IN THE RF CYCLE FOR A 0.5- μ m p^+nn^+ Si DIODE. (OPERATING POINT: $V_{RF} = 14$ V, FREQUENCY = 80 GHz AND $J_{dc} = 10^4$ A/cm 2)

7.5 Conclusions and Program for the Next Quarter. In the preceding sections some results which have been obtained from the large-signal localized avalanche computer program have been presented and discussed. It has been shown that the program can treat diode structures in which a portion of the active region is undepleted. A method has been described for establishing an effective avalanche width by fitting an exact small-signal admittance curve. Large-signal results for an X-band Si diode using this effective avalanche width were found to be in good agreement with another large-signal program which permits distributed avalanche. Results have also been obtained for a millimeter-wave Si diode which show that power and efficiency saturate with voltage drive due to physical processes which occur in the drift region.

During the next period this analysis will be used to study other diode structures and in particular to study GaAs diodes. The effect of lattice temperature upon device performance will also be studied in a systematic way.

8. Solid-State Device Fabrication

Supervisor: N. A. Masnari

Staff: J. East

8.1 Introduction. The objective of this phase of the program is to fabricate IMPATT diodes using the facilities of the Electron Physics Laboratory. Significant progress has been made toward this goal during this reporting period with devices being fabricated from three different types of wafers:

1. nn^+ epitaxial material in which the p^+ layer is formed by diffusion.

2. Double epitaxial p^+ layers on n^+ substrate.
3. pp^+ epitaxial material with the n^+ layer formed by ion implantation of phosphorus ions.

The introduction of integral gold-plated heat sinks has resulted in significant improvement in the quality of the packaged diodes. A large number of diodes have exhibited good thermal resistances as well as powers in excess of 600 mW and efficiencies as high as 6 percent.

3.2 Diode Fabrication. Changes in the fabrication process have been made to improve the thermal resistance of the diodes. Using the process described in Reference 1, the wafer is cleaned, a junction is produced by diffusion or ion implantation and the wafer is thinned and metallized (chrome-gold). It is at this point that significant improvement has been achieved by gold-plating the wafer in a commercial plating solution to produce an integral heat sink. The thickness of the gold plating has varied from 0.001 inch to 0.003 inch.

Several techniques have been used in the plating process. One method is to plate the gold over the entire junction side of the wafer. The substrate side is then covered with an array of small diameter photoresist circles after which the metal not under the dots is etched away. The wafer is then submitted to a silicon etch which removes all of the Si except that under the dots so that the final result is an array of Si mesas attached to the gold-plated layer. The excess gold rims projecting over the Si mesas (a result of undercutting during etching) are removed by subjecting the wafer

1. East, J. and Masnari, N. A., "IMPATT Diode Fabrication," EPL Memo No. 71-1-037250, Electron Physics Laboratory, The University of Michigan, Ann Arbor, 2 June 1971.

to the gold etch once again. Since the tops of the gold caps are protected by the photoresist, the effect is for the etch to attack only the gold rims from underneath. This eliminates the problems experienced in the past of the gold rims folding over and shorting the substrate and junction sides of the diode. The wafer is then separated into individual diodes by cutting the gold plating with a sharp knife or razor blade.

A second method is to use photolithographic techniques to form a pattern of 0.015-inch diameter windows in the layer of photoresist on the junction side of the wafer. The wafer is then waxed to a piece of glass to protect the back and to give mechanical support. When the wafer is inserted into the plating solution only the open windows are plated. After being plated the diodes are formed on the substrate side as described above with the additional precaution that the diodes must be aligned with the gold-plated circles on the junction side. In this case the diodes are separated from each other after the final silicon etch. The individual diodes are then cleaned in an ultrasonic bath sequentially in trichlorethylene, acetone and Freon after which they are baked at 150°C overnight.

The finished diodes vary in diameter from 0.003 inch to 0.005 inch. The first process described above results in the diodes being mounted on square gold-plated pads. In the second process the diodes are located on 0.015-inch diameter gold-plated cylinders. Each unit is then thermo-compression bonded into a package by bringing the bonding tip down around the periphery of the diode, being careful not to touch the diode itself. A 0.003-inch diameter tip is used with 75,000 psi. The heavy pressure ensures a good thermal contact between the package and the integral gold-plated heat sink. There is no danger of damaging the diode at this point

because it is not touched by the bonding tip. After the gold is bonded, a much lighter pressure is used to bond a wire from the top of the diode to the upper flange of the package.

8.3 Experimental Results. A group of 34 ion-implanted diodes was fabricated using the above techniques. The thermal resistances of the diodes with good breakdown characteristics were measured using the standard technique and the definition of thermal resistance as described by Haddad et al.² The average thermal resistance was $21.7^{\circ}\text{C}/\text{W}$ with several being as low as $17^{\circ}\text{C}/\text{W}$. In some cases the diodes were able to withstand 15.5 W of dc power before burnout occurred.

A second group of 19 diodes was fabricated using a double epitaxial wafer. This group had an average thermal resistance of $24^{\circ}\text{C}/\text{W}$. Part of this higher thermal resistance can be explained by the fact that the junction was much deeper in the material.

From the above results it appeared that the thermal resistance had become a secondary problem so three more wafers were fabricated in the hope of improving the RF operation of the diodes. Two of the wafers were from single epitaxial layer material with a 3.5- μm thick, 0.6 $\Omega\text{-cm}$ epitaxial layer. One of these (wafer A) had a 0.5- μm deep diffusion while the other (wafer B) had a 0.7- μm deep diffusion. The third wafer (wafer C) was a double epitaxial wafer ($\text{p}^+ \text{nn}^+$) with the n-layer having a carrier concentration of approximately 10^{16} cm^{-3} . The breakdown voltage of these diodes is approximately 60 to 65 v. Although all of the diodes have not been packaged and tested, several of them from each wafer have been tested for RF

2. Haddad, G. I., Greiling, P. T. and Schroeder, W. E., "Basic Principles and Properties of Avalanche Transit-Time Devices," IEEE Trans. on Microwave Theory and Techniques, vol. MT-18, No. 11, pp. 752-772, November 1970

performance. Diodes from wafer A have averaged approximately 100 mW CW power output in the 6.5 to 8.5 GHz frequency range. Initial tests of diodes from wafer B averaged above 150 mW in the same frequency range. In both cases the bias currents were approximately 90 mA. Recently, two diodes from wafer B have yielded in excess of 600 mW at 6.9 GHz. However, these diodes were rather noisy at these low frequencies while at higher frequencies they were unable to generate more than a few hundred milliwatts.

Diodes from wafer C have yielded power outputs ranging from 100 to 360 mW in the 7.7 to 11 GHz frequency range. A listing of some of these diodes is shown in Table 8.1. It should be mentioned that several of these diodes burned out while tuning because of circuit problems. In particular, most of the difficulty was associated with movement of the center bias conductor during tuning.

Table 8.1
Diodes from Wafer C (Double Ep⁺axial Material)

<u>Diode Number</u>	<u>Bias Current (mA)</u>	<u>Power Output (mW)</u>	<u>Efficiency (%)</u>
1	70	100	1.9
2	55	205	5.0
3	40	110	3.8
4	40	170	5.7
5	40	165	5.5
6	50	210	5.6
7	30	105	4.9
8	50	360	9.8

Following preliminary evaluation of the afore-mentioned diodes, another epitaxial wafer (D) having the same specifications as A and B was diffused to create a deep junction. The diodes fabricated from this wafer are somewhat smaller (~ 0.003 -inch diameter) than the others. At the same time as these diodes were being fabricated, an improved copper collet and heat sink was also constructed. The combination of new diodes and improved heat sink resulted in a vast improvement in the performance of the diodes. Thus far four diodes have been carefully evaluated using the new arrangement. Each diode has generated in excess of 300 mW of power output across the frequency band from 7.4 to 10.6 GHz for bias currents of 130 mA. Figure 8.1 illustrates the power output and efficiency obtained from one of the diodes as a function of frequency for various bias currents. The power output at each bias level extends from 7.8 to 11 GHz. The maximum power of 480 mW at 9.5 GHz is achieved at a bias current of 130 mA. The maximum efficiency of 4 percent also occurs at this point.

Figure 8.2 illustrates an even better performance by a second diode. Again the diode is tunable over a broad frequency range. In addition, it generates a maximum power output of 640 mW at 9.4 GHz for bias current of 130 mA. The maximum efficiency also occurs at this point and is approximately 5.4 percent. It is apparent that both the power output and efficiency have their greatest incremental increase in going from 120 to 130 mA of bias current.

The other diodes had characteristic similar to the above. None of them have been pushed far enough to cause burnout. Based on the measured thermal resistances, it is anticipated that an additional 20 to 30 mA of bias current should be possible without destroying the diodes. Extension of the measurements to the higher bias currents will be implemented as soon as the fabrication of the newly designed copper heat radiating structure is completed.

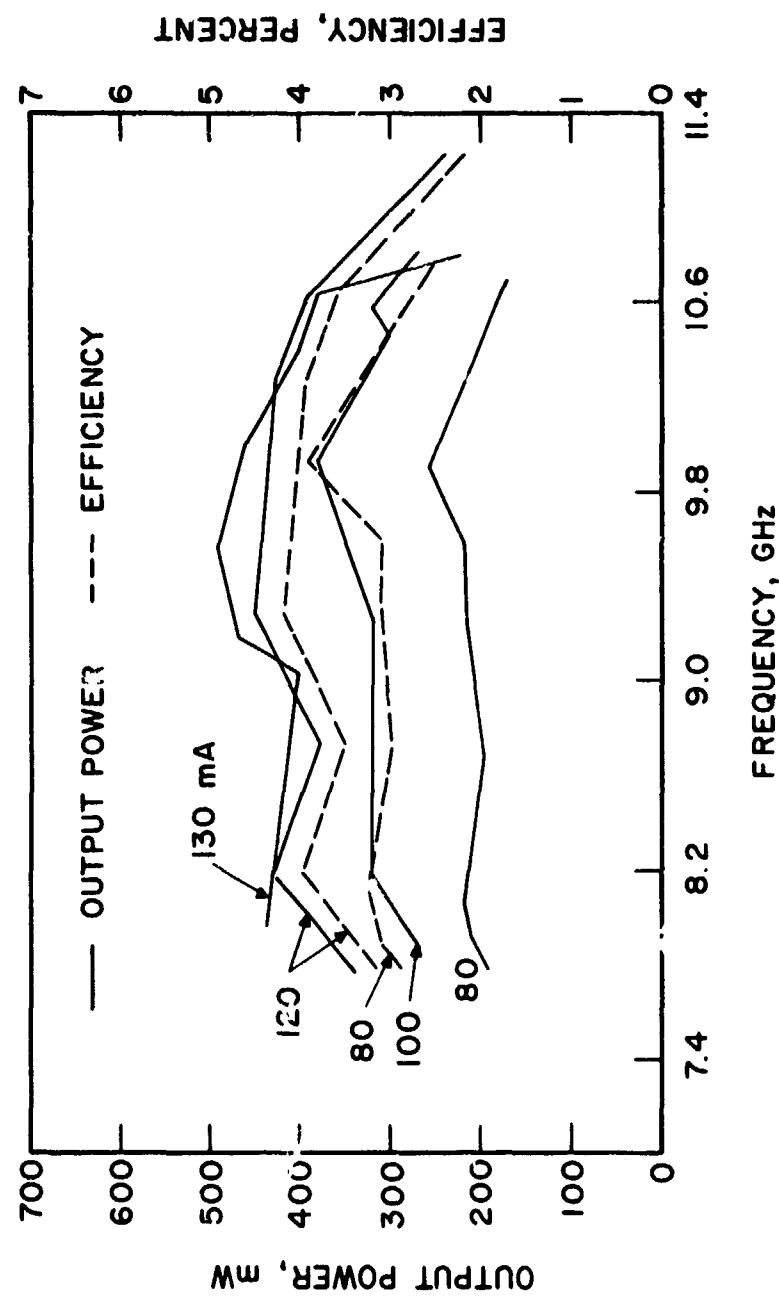


FIG. 8.1 POWER OUTPUT AND EFFICIENCY AS A FUNCTION OF FREQUENCY FOR VARIOUS BIAS CURRENT LEVELS. DIODE 1 FABRICATED FROM WAFER D.

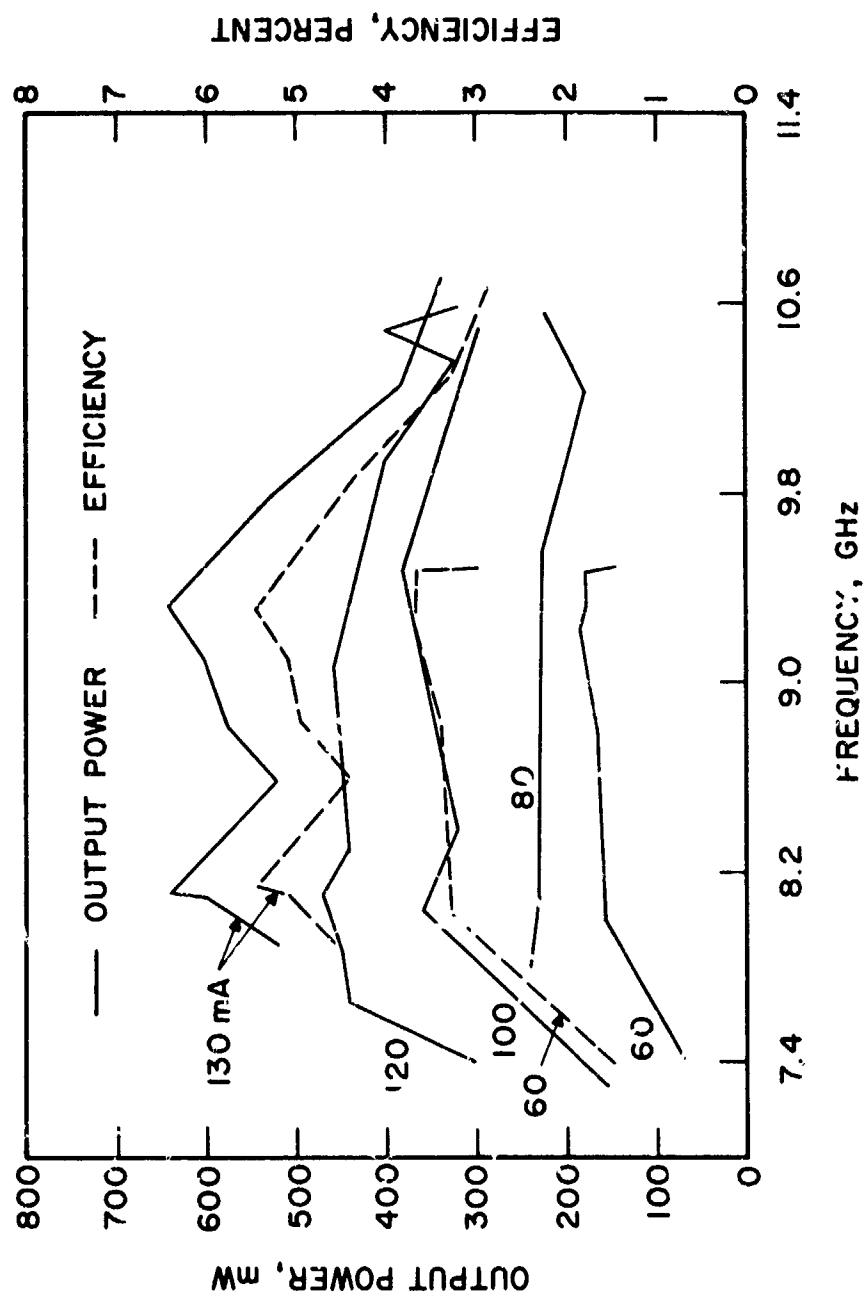


FIG. 8.2 POWER OUTPUT AND EFFICIENCY AS A FUNCTION OF FREQUENCY FOR VARIOUS BIAS CURRENT LEVELS. DIODE 2 FABRICATED FROM WAFER D.

8.4 Conclusions. The fabrication of IMPATT diodes has improved significantly during this reporting period. In particular, the incorporation of the integral gold-plated heat sink has resulted in improved thermal resistance. In addition, the recent acquisition of improved material has also aided in the attainment of better power outputs and efficiencies. Thermal resistances as low as $17^{\circ}\text{C}/\text{W}$ along with maximum power outputs of 600 mW and peak efficiency of 6 percent indicate that the fabrication technique is coming under control.

8.5 Program for the Next Quarter. During the next quarter the remaining diodes from wafers A, B, C and D will be packaged and tested. Also, other wafers will be fabricated to explore the relationship between doping profile and density and the RF operation of the diodes. Now that the power and efficiency appear reasonable, more effort will be devoted to increasing the operating frequency. The primary concern will be with optimization of the circuit to improve the RF performance of the diodes. At the present time the major limitations appear to be associated with the circuit itself.

9. Instabilities in Germanium

Supervisor: J. E. Rowe

Staff: E. H. Sigman

9.1 Introduction. The previous quarterly progress report indicated accuracy problems that were present in the computer subroutine used to calculate collision integrals for the dc model of germanium. This subroutine used the value of the integrand at a few fixed points in the interval of integration to evaluate the integral by Simpson's rule. However, in some cases it was found that the integrand had high amplitude spikes within the range of integration which could cause the Simpson's rule

integration to be inaccurate when only a few fixed points were used.

Modifications have been made to the computer subroutine to alleviate this problem.

9.2 Modifications in the Simpson's Integration Procedure. In order to separate the numerical integration problems from the collision integral subroutine a separate multiple-entry subroutine has been written for the Simpson's integration. The collision integral subroutine has been modified to call on this subroutine as needed. The Simpson's integration subroutine uses a variable step size to achieve the desired accuracy. Since increasing the number of sample points along the entire integration interval would be an inefficient method of improving the accuracy, the subroutine increases the number of sample points only for the portions of the integration interval where it is necessary. This is achieved as follows.

The subroutine starts with five equally spaced points along the integration interval. The value of the integral is calculated from Simpson's rule for five points. The two end points and the midpoint of the interval are then used and the integral value is calculated from Simpson's rule for three points. The three and five point values are compared and if they are within the specified maximum allowable discrepancy the five point value is used for the integral. If the three and five point values are not within the allowable limits then the integrand value is calculated at four new points--the points midway between each pair of previously adjacent points. The integration interval may now be divided in half resulting in five equally spaced points in each half-interval at which the integrand value has been calculated. The three and five point integration values may now be compared in each half-interval. If the desired accuracy has been

attained for a half-interval, the five point value can be used for the half-interval. If the desired accuracy has not been attained, the half-interval can be further subdivided and the same procedure used on each subinterval. In this way extra sample points are taken only in the local vicinity of troublesome points rather than across the entire integration interval.

9.3 Results. The computer subroutine to calculate the integral by Simpson's rule has been implemented and the results have been found to be highly accurate. However in some cases it has been noted that the Simpson's integration subroutine uses over a thousand sample points to calculate the integral. Because of the numerous integrations performed, this quickly leads to excessive computer time for the entire program.

One approach which has been used to alleviate the problem of excessive computer time has been to change the error specification for the Simpson's integration. The accuracy obtained from the variable step size Simpson's integration subroutine is much higher than necessary so that using a less stringent error criterion results in less sample points being required and thus less computer time.

The number of sample points which the Simpson's integration subroutine requires depends upon the smoothness of the function being integrated. In some cases very narrow high amplitude spikes occur in the integrand for the collision integral at the edges of the integration interval due to a degeneracy of the integrand. These spikes can be eliminated by not including the end points in the integration and only approaching the end points close enough to obtain the desired accuracy. This technique can

greatly reduce the number of sample points necessary in degenerate cases while not noticeably affecting the accuracy.

Another factor which has affected the smoothness of the integrand is the use of a tabular method to evaluate the first integrand of the collision integral. This has created a quantization of the integrand with discontinuous steps. It is possible to get around this problem by reversing the order of integrations. A smoother integrand results and the entire program will take less computer time.

9.4 Program for the Next Quarter. The collision integral computer program will be rewritten to change the order of integrations. The computer time for the entire program will be checked in order to keep it within reasonable limits while still maintaining the desired accuracy.